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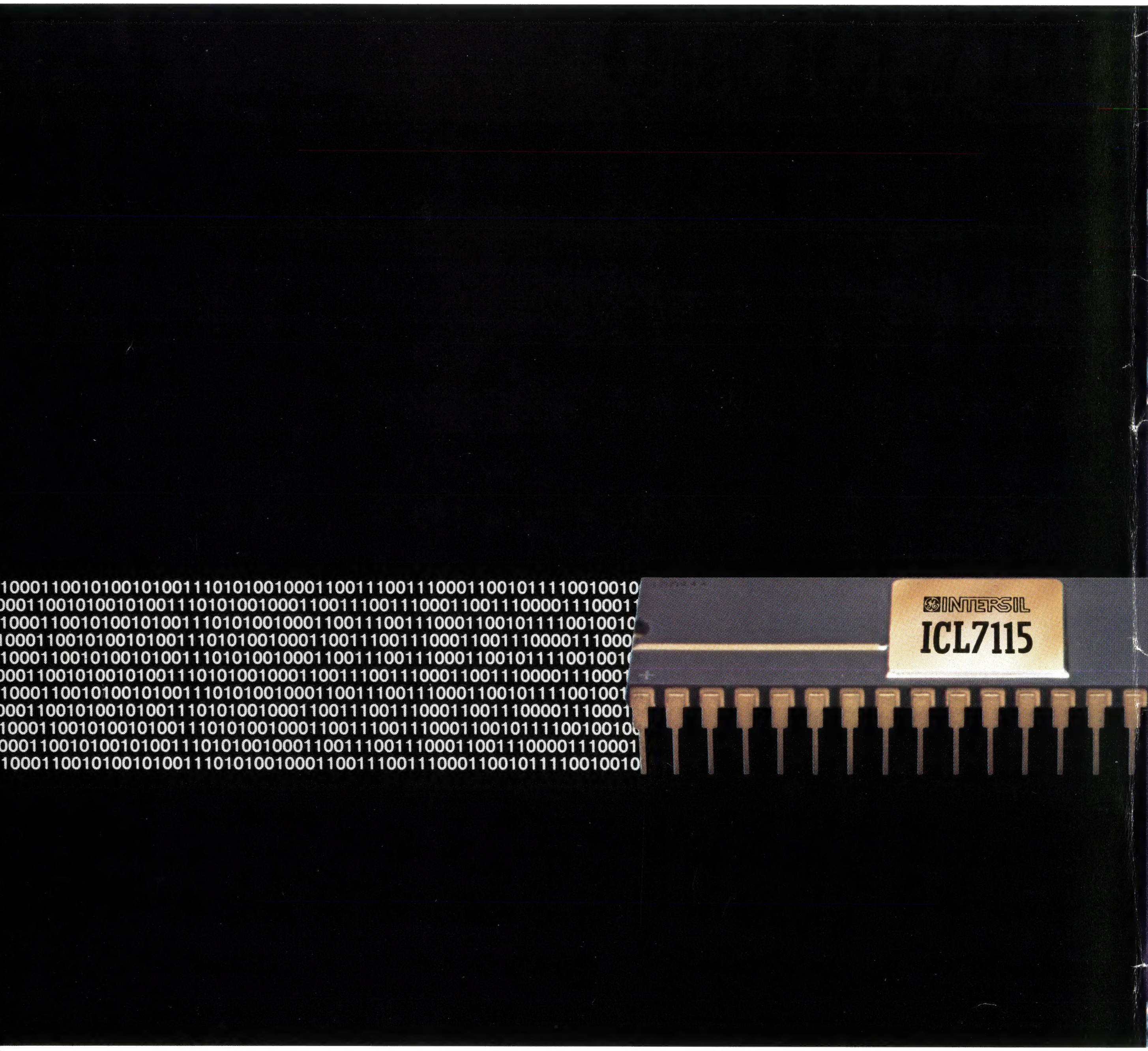
EDN

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

SPECIAL REPORT: BENCHTOP COMPONENT TESTERS

Our ICL7115



The only 14-bit monolithic A/D converter on the market today—that's Intersil's ICL7115. It's the chip that will change the definition of signal processing.

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And if your system requires equal precision in a D/A converter, our ICL7134 meets the challenge. Utilizing the same proprietary EPROM

CIRCLE NO 74

GE stands for Great Engineering in analog signal processing:

Volume 31, Number 6

EDN

March 20, 1986

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: *Benchtop component testers have evolved from simple go/no-go instruments into systems that provide a thorough battery of tests for analog and digital devices. See pg 94. (Photo courtesy Analog Devices)*

DESIGN FEATURES

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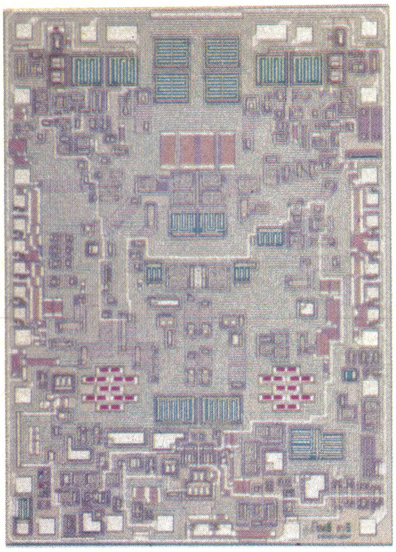
March 20, 1986



***Monolithic instrumentation amplifiers** can help you conserve board space, yet they deliver the performance of their less compact predecessors. You can select either voltage- or current-feedback versions (pg 57).*

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

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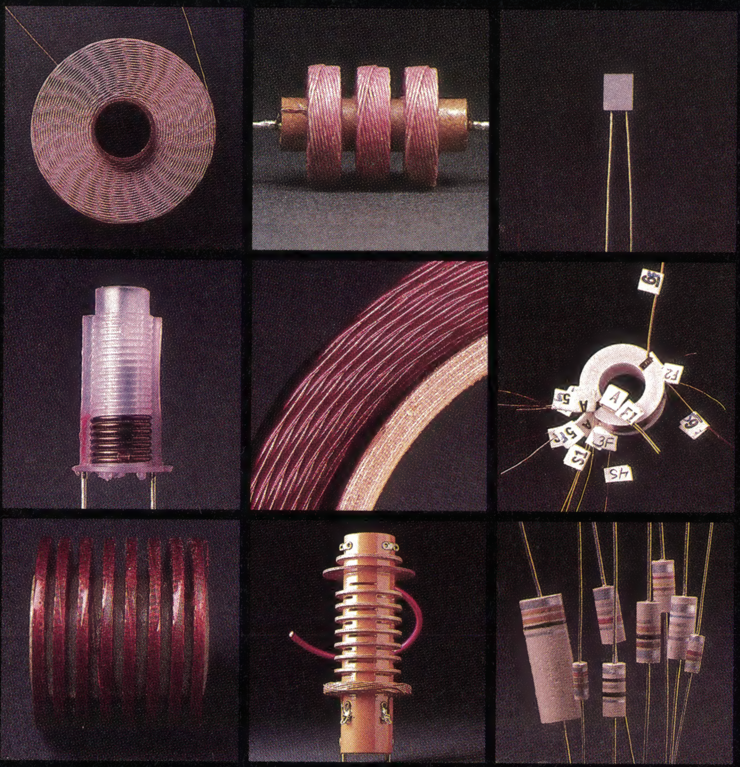

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BELL INDUSTRIES

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Beginning next month, EDN will provide another tool that will help you evaluate new products quickly and effectively—EDN *Product News*. The product articles contained in this tabloid-size publication, combined with EDN's applications-oriented coverage, will give you the most comprehensive package of engineering information currently available.

NEW PRODUCTS

PROFESSIONAL ISSUES

LOOKING AHEAD 331

Personal-computer market to grow slowly in 1986 . . . Databases to streamline infrastructure management.

DEPARTMENTS

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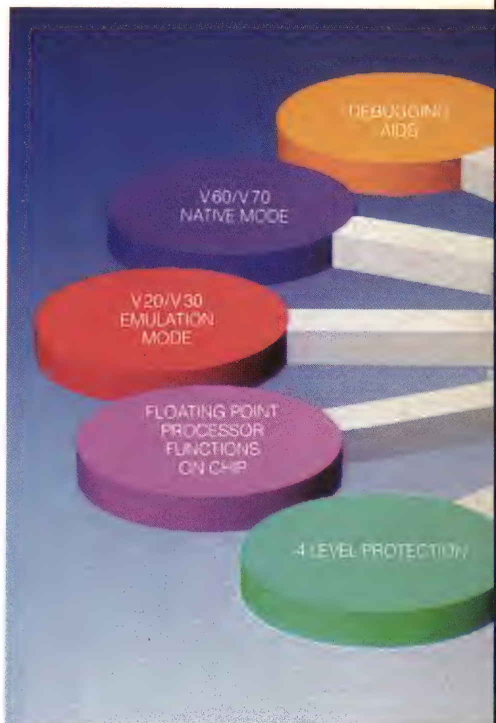
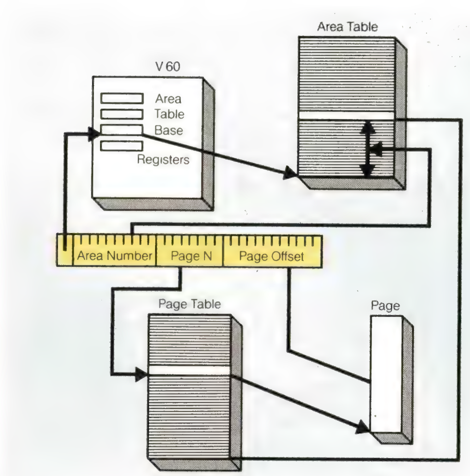
Leading

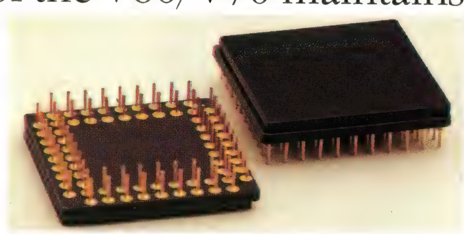
The new



V60/V70 – Revolutionary advances in CMOS technology for the ultimate 32-bit microprocessor performance. NEC's new supermicro family is based on a general purpose architecture with a whole arsenal of on-chip features to handle the most sophisticated and complex applications in industrial control, office automation and telecommunications.



NEC's proprietary CMOS VLSI technology, which packs more than 375.000 transistors on a single chip and achieves extremely low power consumption, is the key to performance. The V60 has an external 16-bit bus while the V70 is a full 32-bit machine. With a six-stage pipeline structure, both are designed for high throughput, performing at 3.5 and 5.3 MIPS (MAX) respectively. On-chip floating point functions provide the extra zip demanded by compute-intensive applications.



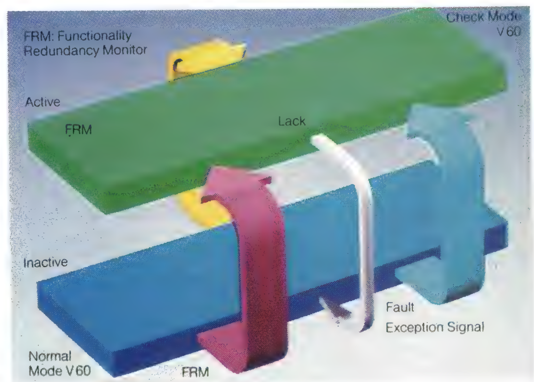
The on-chip memory management unit of the V60/V70 maintains a mammoth 4 Gigabyte virtual address space and a four-level protection mechanism for efficient implementation in multi-user environments. The processors can operate in native mode or 16-bit V20/V30 emulation mode, demonstrating yet again the fundamental compatibility strategy of the entire V-Series.

the field

V-Series.

V60/V70
32-BIT SUPER
MICROPROCESSORS

A powerful chip feature of the V60/V70 is the unique functional redundancy monitor. This feature allows the design of highly reliable, fault tolerant systems by putting together two or more processors to operate in parallel. Validity of outputs of these is automatically checked every machine cycle for early detection and possible correction of the System operations.



Hardware expandability for the V60/V70 is assured by the full line of compatible CMOS peripheral devices. Software power comes from the V60/V70 instruction set, ideally suited for high-level language support and compiler optimization. An on-chip debug facility cuts down development time by efficient on-line error detection. Standard V60/V70 operating software includes *UNIX V and NEC's own Real-Time Operating System.

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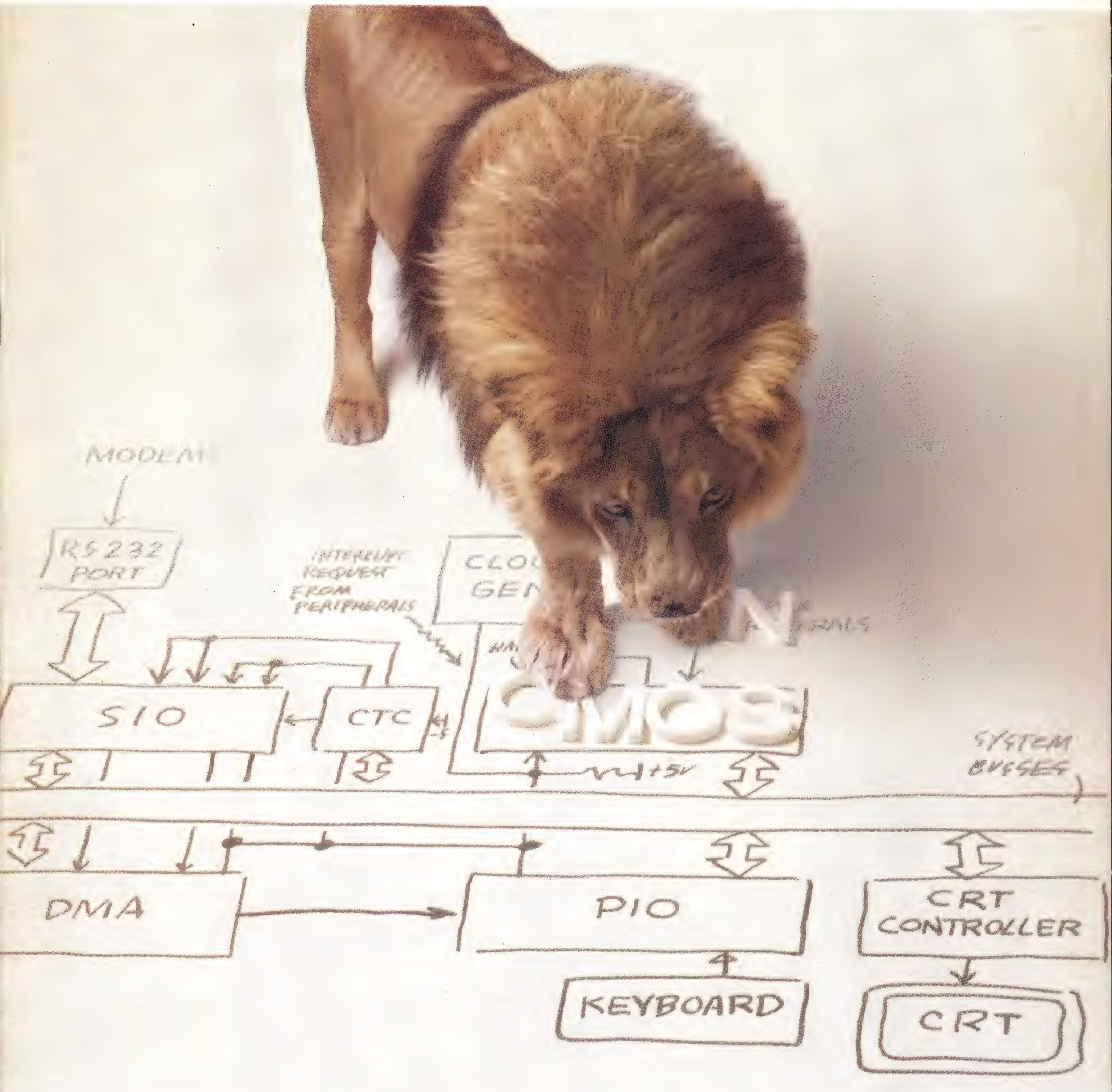
TOSHIBA CMOS



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NEWS BREAKS

EDITED BY JOAN MORROW

C-LANGUAGE SYMBOLIC DEBUGGER RUNS ON IBM PC

The DE-1000 universal μP development system from Emulogic (Norwood, MA) works with a variety of host computers and features Slice—a high-level symbolic debugger for the C programming language. The Slice debugger lets you examine and modify both local and global variables, trace C function calls and stack usage, and evaluate expressions in C or assembly language. In addition, you can track the movement of variables between registers and stack, examine functions in C or assembler, and step your program by source line, call, assembler instruction, or bus cycle. The emulator works with 68000 and 8086 target systems. You can use any IBM PC or any level VAX—including a MicroVAX—as a host. The DE-1000 costs $12,000 for the IBM PC version and $16,000 for the VAX version.—Charles H Small

24-PIN PLD IS ELECTRICALLY ERASABLE

The GAL 20V8 from Lattice Semiconductor (Beaverton, OR) is the first electrically erasable 24-pin PLD. Electrically erasable PLDs require less time and equipment to reprogram than do erasable PLDs that require ultraviolet lamps to erase. The GAL 20V8 contains programmable macrocells that allow it to replace any of 20 types of 24-pin PLDs. Its 25-nsec propagation delay makes it as fast as many bipolar parts, but the device consumes 50% less power (90 mA vs 180 mA for bipolar devices). The output circuits can sink 24 mA, which guarantees compatibility with bipolar PLDs. The GAL 20V8 costs $17.63; a 35-nsec version costs $13.26 (100).—David Smith

SEVERAL NONVOLATILE MEMORY ICs OFFER GREATER SPEED, DENSITY

Several chip manufacturers have recently released EPROM and EEPROM chips with improved speed and density. Atmel Corp's (San Jose, CA, (408) 434-9201) AT28C64, a CMOS 64k-bit (8k-byte) EEPROM with 100,000 write/erase cycles, features a self-timed write cycle of 200 μsec max and an access time of 150 nsec. Such write speeds are at least 10 times faster than those exhibited by conventional EEPROMs. In standby mode, the part draws only 10 μA from one 5V supply and requires no more than 10 mA in the active mode. The AT28C64 costs $42.10 (100) in 28-pin ceramic DIPs or 32-pin LCCs.

Xicor Inc (Milpitas, CA, (408) 946-6920) has begun sampling its 256k-bit (32k-byte) X28256 EEPROM. The part incorporates a 28-pin DIP footprint that allows upgrades from designs previously employing standard 64k-bit EEPROMs. The device delivers a 150-nsec access time and a 2-msec page-write time; active supply current from one 5V power source is less than 100 mA. Production quantities of the X28256 will be available in April for $120 (100).

Intel Corp's (Folsom, CA, (916) 351-2746) high-speed 27128B-110/05 128k-bit EPROM features a maximum access time of 110 nsec, which represents a 40-nsec improvement over their previous high-speed 27128A-1 EPROM. In a JEDEC-approved, 28-pin windowed ceramic DIP, the device costs $13.30 (1000).

Production quantities of the CMOS Am27C1024 1M-bit (65,536x16-bit) EPROM from Advanced Micro Devices (Sunnyvale, CA, (408) 732-2400) are now available in a 40-pin DIP for $199 (100). Despite its high density, this EPROM features interactive block-programming algorithms and typical access times of 200 nsec.—Denny Cormier

STE BUS DEVELOPMENT SYSTEMS SUPPORT 68008 AND 64180 DESIGNS

Performance Interconnect Inc (La Jolla, CA, (619) 457-0665) offers development systems for the STE Bus. The PII-DS-S1 and PII-DS-S2 systems include Hitachi 64180 and

Motorola 68008 CPU boards, respectively. Each system also includes dual 3½-in., 1M-byte floppy-disk drives and a 20M-byte Winchester drive. The systems leave seven STE Bus slots empty for customization. The 64180 system runs CP/M+ or ZRDOS; the 68008 environment employs the multiuser, multitasking PDOS operating system. Each system with software costs $4995.—Maury Wright

HIGH-LEVEL META-ASSEMBLER DETECTS ERRORS

The MetaStep program from Step Engineering (Sunnyvale, CA) is a retargetable, relocatable, macro meta-assembler. You can produce small modules of microprogramming—rather than write your microprogram as a monolithic whole—and later link the modules together to suit the target. Unlike earlier meta-assemblers written in Fortran, MetaStep was written in C and features C-like, free-form definition of microcode operators. You can also build in range checking and other programmer constraints. MetaStep assembles at more than 10,000 fields/minute and also processes AMDASM source code.—Charles H Small

AI DEVELOPMENT SYSTEM RUNS ON IBM PC/AT

You can develop Lisp-based artificial-intelligence software on an IBM PC/AT by using the $1195 GCLISP 286 Developer from Gold Hill Computers (Cambridge, MA, (617) 492-2071). This development system includes a memory interpreter, a compiler, an editor, a tutorial, and on-line help features for creating programs written in Golden Common Lisp. Running under PC-DOS version 3.0, the software can address as many as 15M bytes of physical memory. It requires at least 2M bytes of memory, a floppy-disk drive, and a hard disk.—David Smith

ICs ENSURE SYSTEM INTEGRITY DURING POWER FAILURES

Providing orderly shutdown and automatic restart for μP-based systems, the Integrated Battery Backup from Dallas Semiconductor Corp (Dallas, TX, (214) 450-0400) is a 3-part chip set that protects critical data during a power loss. This chip set allows your system to restart a task where it stopped, as if no power disruption had occurred. The first chip, the DS1231, is a power monitor that warns the system's μP of a possible power failure, thus allowing the μP to store critical data before a power loss. The DS1260 supplies battery power to your volatile RAMs when line voltage falls below a critical level. The DS1212 determines whether the line voltage or the battery will best maintain the RAM data. The DS1231 costs $3.30; the DS1260 starts at $6.25; and the 16-RAM DS1212 costs $6.70 (1000).—J D Mosley

CHOPPER-STABILIZED OP AMP WORKS FROM ±15V SUPPLIES

The TSC915 operational amplifier from Teledyne Semiconductor (Mountain View, CA, (415) 968-9241) operates from supply voltages ranging from ±3.5V to ±16V. Monolithic chopper-stabilized op amps have traditionally imposed power-supply limits of ±7.5V. The TSC915 uses a metal-gate CMOS process; its chopper stabilization holds offset voltage to 10 μV max with drift of 0.1 μV/°C. Input bias and offset currents are 100 pA max. Common-mode rejection, power-supply rejection, and open-loop gain are all 140 dB typ. Permissible common-mode range for the input extends from the negative supply to within 2V of the positive supply. Input noise is 0.2 μV p-p over a 0.1- to 1-Hz bandwidth, unity-gain bandwidth is 500 kHz, and slew rate is 0.5V/μsec. Prices for commercial- and industrial-range devices are $4.50 and $5.60 (100), respectively.—Bill Travis

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Whether your needs are for medical, seismic, radar, image processing, or general data conversion applications, TRW LSI's leading-edge technology provides A/D converters for your specific digital signal processing function, word size and speed requirements.

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TRW Electronic Components Group

NEWS BREAKS: INTERNATIONAL

BY PETER HAROLD

VME BUS IEEE-488 CONTROLLER SUITS FUNCTIONAL PARTITIONING

The PME68-14 board comes with a 68000 or 68010 μP, as much as 2M bytes of dual-ported RAM, and an interface and driver firmware for IEEE-488 bus control. From Plessey Microsystems (Towcester, UK, TLX 31628), the board is suited for use as an intelligent IEEE-488 subsystem in VME Bus systems or as a stand-alone IEEE-488 controller. Based on the TMS9914 IEEE-488 interface IC, the double Eurocard board has full talker, listener, and system-controller capabilities. Sockets are provided for as many as four 28-pin EPROM/static RAMs and for a DMA controller. Additional onboard functions include two serial ports, a real-time clock calendar, and three 16-bit counter/timers. The board's VME Bus interface includes slot 1 system-controller functions; its P2 connector carries a buffered 68000 bus for expansion purposes. With 512k bytes of dual-ported RAM, the board sells for less than £1000.

ADD-IN BOARD TRANSFORMS PC INTO SEMIGRAPHICS TERMINAL

Suited for use in IBM PC, PC/XT, PC/AT and compatible computers, the USGT/PC card from Devlonics Terminals NV (Kortrijk, Belgium, TLX 85643) allows you to communicate with a variety of videotex and TTY-based information sources via its onboard autoanswering V21/V23 modem. A Bell-standard modem version is also available. The board supports Prestel and Teletel videotex standards. The software includes a videotex and TTY editor and PC-to-PC file-transfer utilities. Autodial facilities include automatic selection of pulse or tone dialing. You can program as many as 10 menu-selected automatic dial-up sequences. In addition, the board provides the PC with an additional RS-232C interface. Including diskette-based software for the PC, the USGT/PC costs Bfr 43,000.

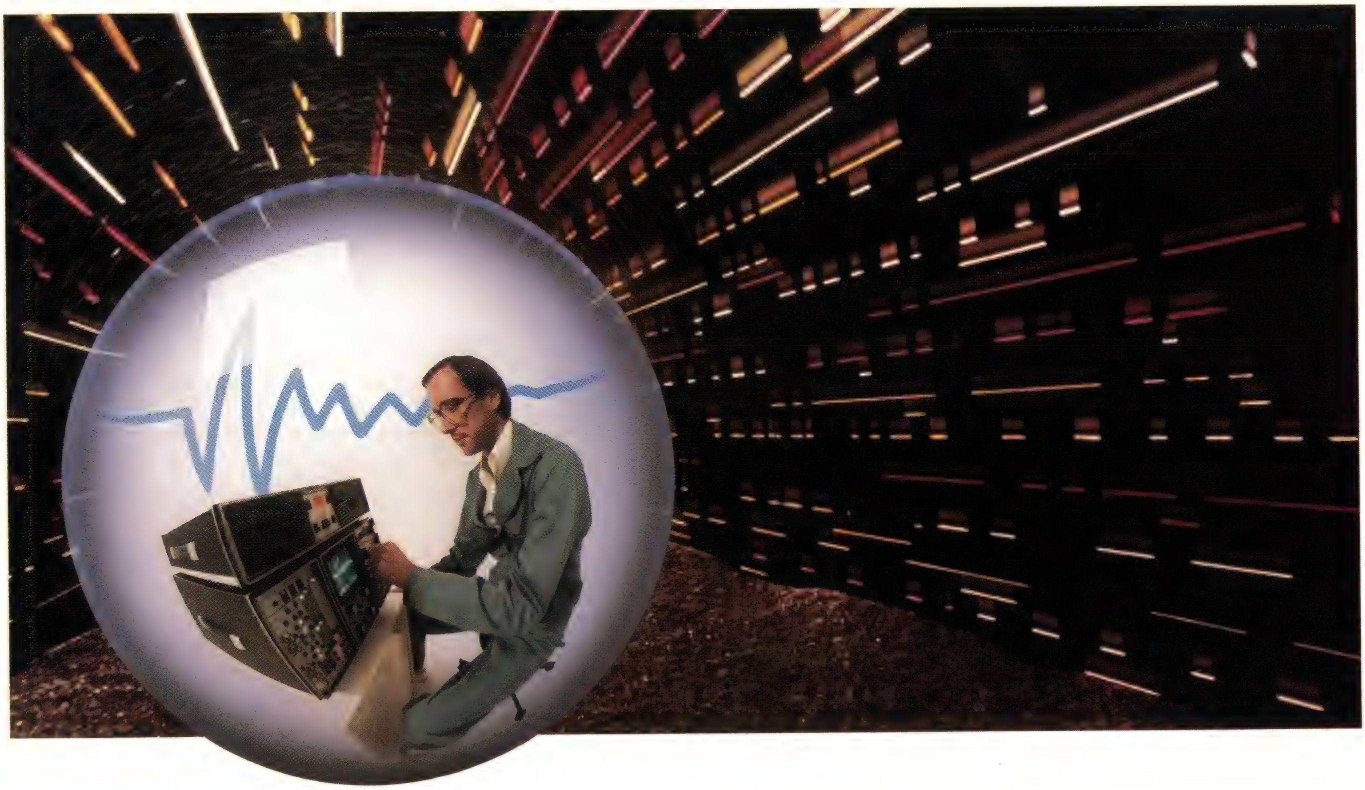
CCD IMAGE SENSORS FEATURE ANTIBLOOMING FUNCTION

The P86000 and P85000 Series monochrome, CCD frame-transfer image sensors feature antiblooming circuitry to prevent pixel overloads. Options include front or back face illumination. Manufactured by EEV Ltd (Chelmsford, UK, TLX 99103), the 288×385-pixel P86000 Series serves 625-line TV picture generation; the 244×385-pixel P85000 Series is intended for dedicated 525-line applications. Both series, which should be available in May, have a ⅔-in. format, and devices with ½-in. format will be available by the third quarter. A range of hybrid support circuits provides drive logic and peripheral functions including CCIR or EIA video output, automatic gain control, and blemish correction.

A/D VME BUS BOARD FEATURES INDIVIDUAL CHANNEL PROGRAMMING

The AD12VME-16 and -32 VME Bus A/D-converter cards from Anglia Technology Ltd (Norwich, UK, TLX 975646) provide 16 or 32 analog input channels, respectively, which you can individually program for input range and for single-ended or differential, unipolar or bipolar operation. The board has an overall system accuracy of 0.024% on all of its input ranges from 100 mV to 10V full scale, a resolution of 12 bits, and a maximum throughput rate of 28k samples/sec. It also provides 500V isolation between the input and VME Bus grounds. The 16-channel board costs £1395, and the 32-channel version costs £1520.

THE FIRST NAME IN DIGITAL SCOPES



TIME MACHINES.

The Past. Nicolet digital oscilloscopes can record the history of your signal before the trigger point. Examine what preceded an event as well as the event itself. Use expansion to analyze the signal in detail at up to 100 times the resolution of an analog scope. Store the signals on floppy disk or bubble memory for future recall and reference. Or plot them out in report ready format.

The Present. Compare live signals with each other or with previously stored signals. Store any signal with the touch of a button and use voltage and time numeric display for exact comparisons. You can even display related signals as functions of each other instead of time. Manipulate waveforms using the scope's built-in programs or transmit them to a computer and back for display.

The Future. Expecting a transient? Set-up your Nicolet scope to capture it while you're away! Some models can even capture a sequence of events and store them on disk or bubble memory automatically ready for instant recall and display.

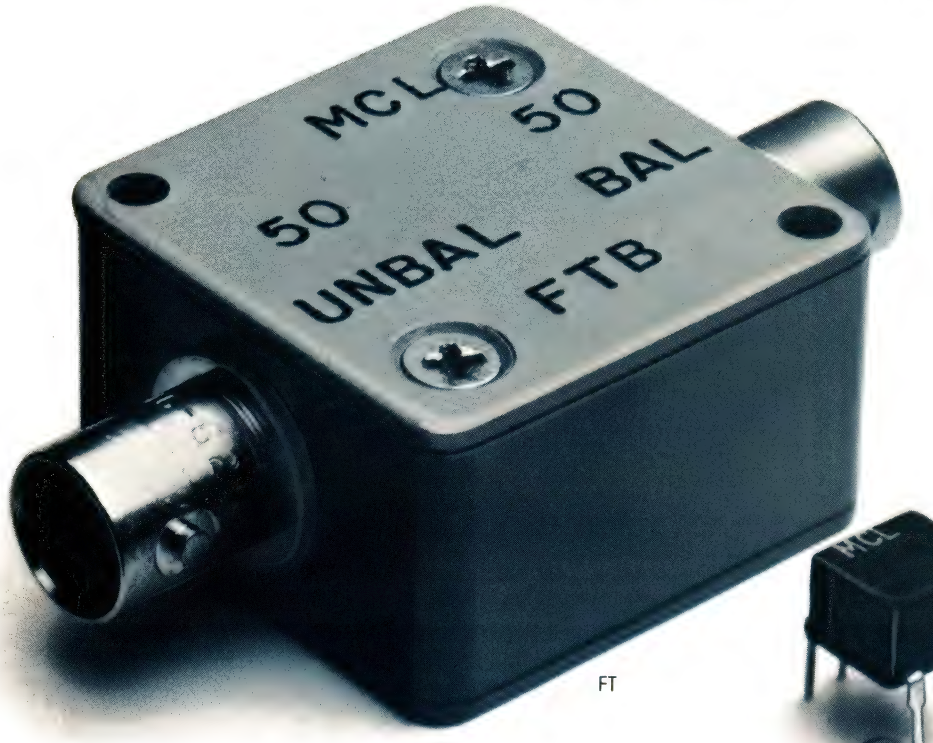
Get Results First Time, Everytime. Don't miss important data because of set-up error. Nicolet scopes are easy to use. Find out how they can be the quickest solution to your signal problems. For more information, write Nicolet Oscilloscope Division, 5225 Verona Road, Madison, WI 53711. Or call 608/273-5008.

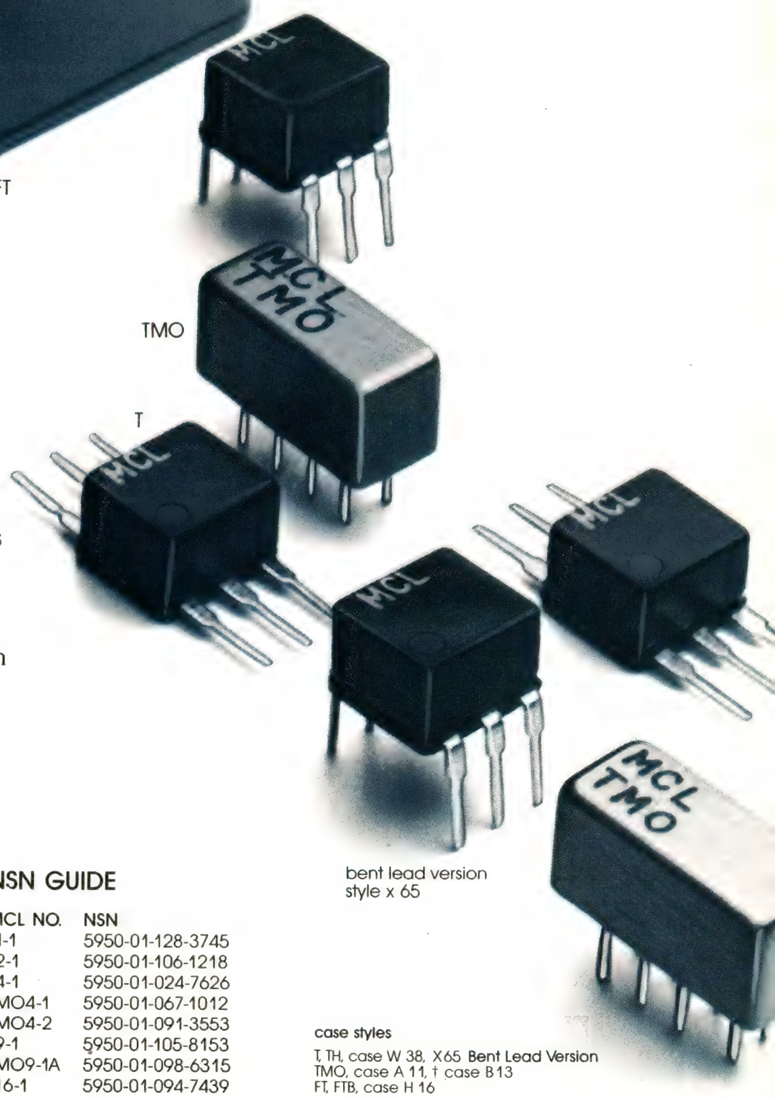
Nicolet

For more information circle 10

RF trans

over 50 off-the-shelf models...





Having difficulty locating RF or pulse transformers with low droop, fast risetime or a particular impedance ratio over a specific frequency range?...Mini-Circuits offers a solution.

Choose impedance ratios from 1:1 to 36:1, connector or pin versions (plastic or metal case built to meet MIL-T-21038 and MIL-T-55831 requirements*). Ultra-wideband response achieves low droop and fast risetime for pulse applications. Ratings up to 1000M ohms insulation resistance and up to 1000V dielectric voltage. For wide dynamic range applications involving up to 100 mA DC primary current, use the T-H series. Coaxial connector models are offered with 50 and 75 ohm impedance; BNC standard; request other types. Available for immediate delivery with one-year guarantee.

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*units are not QPL listed

NSN GUIDE

MCL NO.	NSN
T1-1	5950-01-128-3745
T2-1	5950-01-106-1218
T4-1	5950-01-024-7626
TMO4-1	5950-01-067-1012
TMO4-2	5950-01-091-3553
T9-1	5950-01-105-8153
TMO9-1A	5950-01-098-6315
T16-1	5950-01-094-7439

case styles

T, TH, case W 38, X65 Bent Lead Version
TMO, case A 11, † case B13
FT, FTB, case H 16

finding new ways...
setting higher standards

Mini-Circuits

A Division of Scientific Components Corporation
World's largest manufacturer of Double Balanced Mixers
P.O. Box 166, Brooklyn, New York 11235 (718) 934-4500
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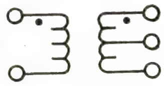
C72-1 Rev. A

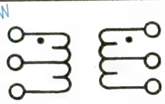
formers

3KHz-800 MHz from $2^{95}

CAPD now available! computer-automated performance data

case style number see opposite page.

A*


B* NEW


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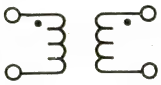

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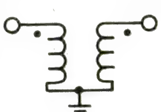
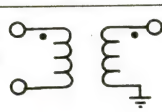


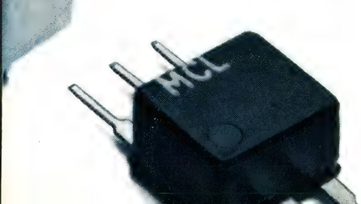
E


Case	Type	MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	INSERTION LOSS 2dB MHz	INSERTION LOSS 1dB MHz	PRICE $ Ea.	PRICE $ Qty.
A*	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	3.95	(10-49)
		T1-6T NEW	1	.003-300	.003-300	.01-150	.02-50	5.95	(10-49)
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.25	(10-49)
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	4.25	(10-49)
		T3-1T	3	.05-250	.05-250	.1-200	.5-70	3.95	(10-49)
		T4-1	4	.2-350	.2-350	.35-300	2-100	2.95	(10-49)
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	3.95	(10-49)
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.25	(10-49)
		T8-1T	8	.03-140	.03-140	.10-90	1-60	6.95	(10-49)
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.25	(10-49)
		T16-6T NEW	16	.03-75	.03-75	.06-30	.1-20	4.95	(10-49)
	TH	T4-1H	4	8-350	8-350	15-300	25-200	4.95	(10-49)
	TMO	TMO1-1T	1	.05-200	.05-200	.08-150	.2-80	6.45	(10-49)
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	6.75	(10-49)
		† TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	6.75	(10-49)
		† TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	6.45	(10-49)
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	4.95	(10-49)
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	6.75	(10-49)
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	6.75	(10-49)
B* NEW	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	5.95	(10-49)
		TT1.5-1	1.5	.075-500	.075-500	.2-100	.1-50	4.95	(10-49)
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	5.25	(10-49)
		TT4-1	4	.05-200	.05-200	.02-50	1-30	4.95	(10-49)
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	7.95	(10-49)
	TTMO	TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	10.95	(10-49)
C	T	T1-1	1	.15-400	.15-400	.35-200	2-50	2.95	(10-49)
		T1-6 NEW	1	.01-150	.01-150	.02-100	.05-50	4.95	(10-49)
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	3.95	(10-49)
		T1.5-6 NEW	1.5	.02-100	.02-100	.05-50	0.1-25	4.95	(10-49)
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	3.95	(10-49)
		T4-6	4	.02-200	.02-200	.05-150	.1-100	3.95	(10-49)
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.45	(10-49)
		T16-1	16	.3-120	.3-120	.7-80	.5-20	3.95	(10-49)
		T36-1	36	.03-20	.03-20	.05-10	.1-5	5.95	(10-49)
	TH	T1-1H	1	8-300	8-300	10-200	25-100	4.95	(10-49)
		T9-1H	9	2-90	2-90	3-75	6-50	5.45	(10-49)
		T16-1H	16	7-85	7-85	10-65	15-40	5.95	(10-49)
	TMO	TMO1-1	1	.15-400	.15-400	.35-200	2-50	4.95	(10-49)
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	6.75	(10-49)
		† TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05.20	6.45	(10-49)
		† TMO4-6	4	.02-200	.02-200	.05-150	.1-100	6.45	(10-49)
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	6.45	(10-49)
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	6.45	(10-49)
		TMO1.6-1	16	.3-120	.3-120	.7-80	5-20	6.45	(10-49)
D	T	T2-1	2	.025-600	.025-600	.05-400	.5-200	3.45	(10-49)
		T3-1	3	.5-800	.5-800	.2-400	—	4.25	(10-49)
		T4-2	4	.2-600	.2-600	.5-500	.2-250	3.45	(10-49)
		T8-1	8	.15-250	.15-250	25-200	2-100	3.45	(10-49)
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.25	(10-49)
	TMO	TMO2-1	2	.025-600	.025-600	.05-400	.5-200	5.95	(10-49)
		TMO3-1	3	.5-800	.5-800	2-400	—	6.95	(10-49)
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	5.95	(10-49)
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	5.95	(10-49)
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	6.75	(10-49)
E	FT	FT1.5-1	1.5	.1-400	.1-400	.5-200	1-100	29.95	(1-4)
	FTB	FTB1-1	1	.2-500	.2-500	.5-300	10-100	29.95	(1-4)
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	29.95	(1-4)
		■ FTB1-1-75	1	.5-500	.5-500	5-300	10-100	29.95	(1-4)

■ Denotes 75 ohm models

* Maximum Amplitude Unbalance
0.1 dB over 1 dB frequency range
0.5 dB over entire frequency range

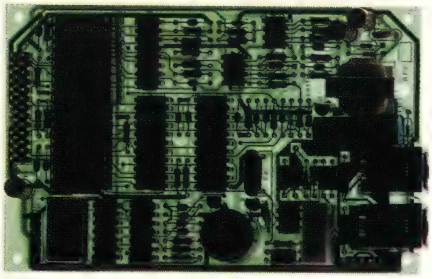
* Maximum Phase Unbalance
1.0° over 1 dB frequency range
5.0° over entire frequency range



C72-2 Rev. A

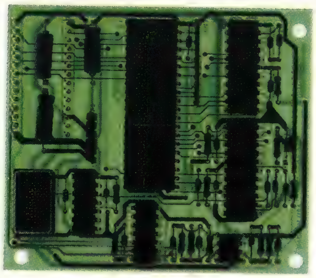
CIRCLE NO 81

When you positively custom



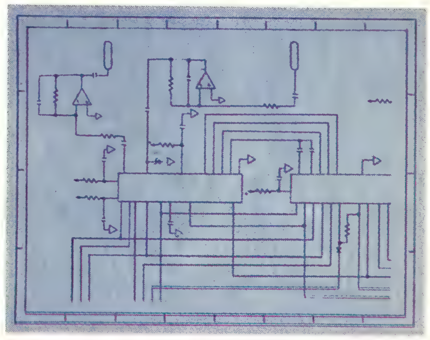
Reliability

is your obvious first requirement in this vital link between your product and the outside world. At Ven-Tel—with 12 years experience and millions of modems designed and shipped—we don't take reliability for granted...*so you can.*



Compatibility

with industry standards. All Ven-Tel modems utilize the industry standard "AT" command set, guaranteeing compatibility with virtually all types of software. And every Ven-Tel custom modem is fully compatible with our complete line of standard desktop and PC internal modems. We also meet Bell 212A and CCITT V.22bis standards in speeds up to 2400 baud.



Quick Turnaround

is more than a phrase to us. We've built a reputation for meeting product deadlines among some of the nation's largest and most demanding manufacturers. From start to finish in as little as 90 days, Ven-Tel can help you get your product to market quickly. You can even begin development using our standard modules while your design is being finalized.

take a good

Our new Opto
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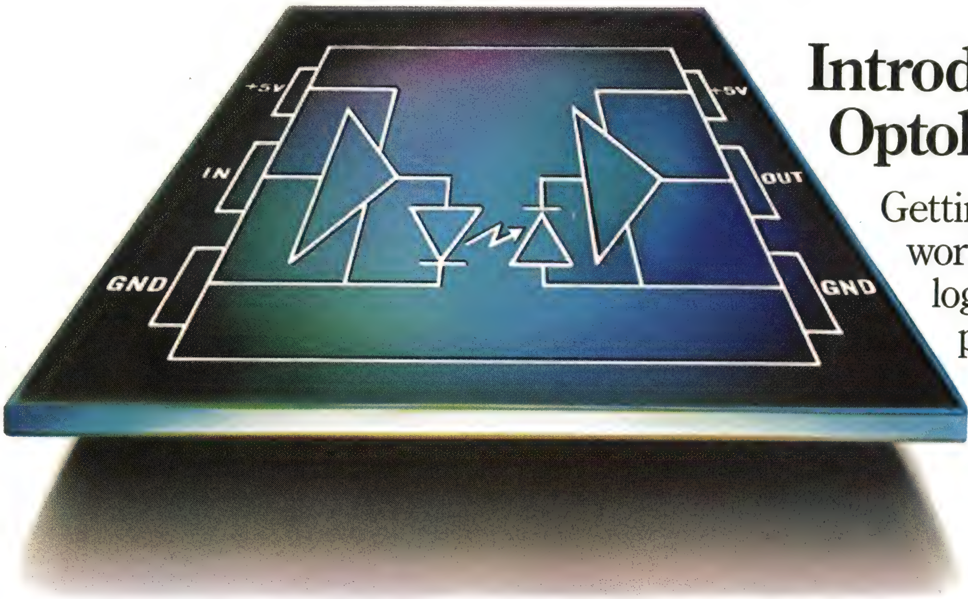


Introducing the Optologic™ Coupler.

Getting lost in the analog world is no fun for the logic designer. In the past you had to consider trade-offs between input current, LED temperature dependence, speed and many other parameters. Many of these trade-offs were figured out by trial and error. It was really time consuming. And a real pain. But now there's good news ahead.

A new concept.

Now you can achieve optoisolator protection without having to understand the analog operation of the optocoupler.

The Optologic coupler is the first general purpose, high speed optoisolator that looks exactly like any common 74-series logic gate at both input and output. This makes it extremely easy to interface between same or different logic families. The innovative use of an input amplifier ensures real LSTTL compatibility and preserves your TTL noise immunity.

The Optologic coupler will find wide use in data communications. In local area networks you can greatly improve noise immunity while utilizing the device's high input impedance in multiple bridged line receivers.

The Optologic coupler is available from these distributors:

U.S.

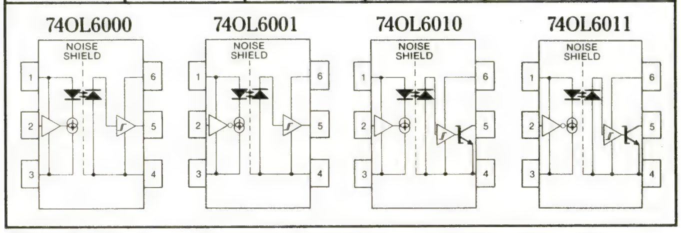
ARROW ELECTRONICS, INC.
BELL INDUSTRIES
(GRAHAM DIVISION)
CAM/RPC
HAMMOND ELECTRONICS, INC.
HARRISON EQUIP. CO., INC.
J.V. ELECTRONICS
KIERULFF ELECTRONICS
MILGRAY ELECTRONICS, INC.
NEWARK ELECTRONICS
SCHWEBER ELECTRONICS
SUMMIT DISTRIBUTORS, INC.
WYLE LABORATORIES

isolator thinks gital IC.

In another common application, AC/DC precision level sensing is possible because of the well-defined input threshold.

And the price is competitive with other high speed optocouplers.

PART NUMBER	LOGIC COMPATIBILITY		LOGIC FUNCTION	OUTPUT CONFIGURATION
	INPUT	OUTPUT		
74OL6000	LSTTL	TTL	BUFFER	TOTEM POLE
74OL6001	LSTTL	TTL	INVERTER	TOTEM POLE
74OL6010	LSTTL	CMOS	BUFFER	OPEN COLLECTOR
74OL6011	LSTTL	CMOS	INVERTER	OPEN COLLECTOR



There are two output versions available: one with totem pole circuit configuration for TTL compatibility, and another with open collector for interface to 4.5 V to 15 V CMOS or power transistors.

High performance and reliability.

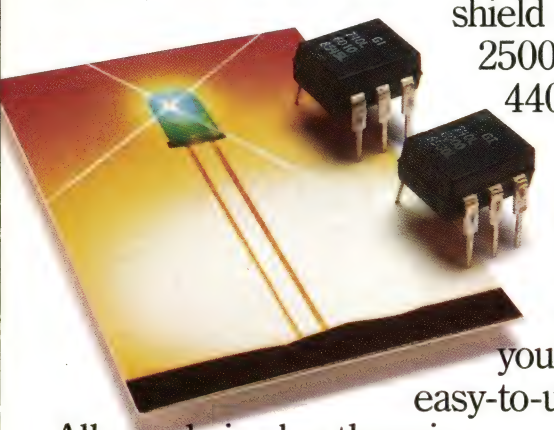
Propagation delay of the Optologic coupler is 60ns and supports datacom to 15 MBaud. The built-in internal noise shield offers 15kV/μs common mode transient rejection.

2500 VAC RMS isolation for one minute corresponds to a 440 VAC working voltage.

MTTF is 1.68 million hours at 90% confidence.

The Optologic coupler is a fool-proof device that provides a level of design integrity and security that the engineer has not had before.

If you hate leaving the digital world every time you want to optically isolate your circuits, design in the easy-to-use Optologic couplers from the LightHouse.



All you do is plug them in.

And bingo.

For samples or information about immediate volume production, contact your local distributor or General Instrument, Optoelectronics Division, 3400 Hillview Avenue, Palo Alto, CA 94304. (415) 493-0400. TWX: 470208.

GENERAL INSTRUMENT
Optoelectronics Division

The LightHouse you can depend on.

CIRCLE NO 83

CANADA

ARROW	CARDINAL INDUSTRIAL ELECTRONICS	FUTURE ELECTRONICS, INC. RAE ELECTRONICS


LEADER

SIGNALS & NOISE

IEEE survey covered numerous topics

Dear Editor:
With reference to your editorial "IEEE's rosy picture hides thorns," (EDN, December 12, 1985, pg 51), I would like to make several comments. First, it should be noted that the IEEE survey apparently being cited (and compared adversely to an EDN survey) is the *US Member Opinion Survey 1985*. The editorial suggests that the Member Opinion Survey concentrated entirely on job satisfaction. The survey actually covered numerous topics, including public policies, ethics, career maintenance and development, and education. Job satisfaction was one of five subtopics in the section on career maintenance and development.

I would also like to point out that the professional consultant who worked with the Member Opinion Survey committee in producing the survey tells me that there's no such thing as "a true neutral response." She suggests that "neutral is not neutral." Similarly, the term "moderately satisfied" implies at least some dissatisfaction. It seems to be your conclusion, not the Member Opinion Survey's, that the first three scales (out of five) can be added together to indicate 90% job satisfaction.

Another IEEE survey, conducted by Spectrum/Harris, states: "Nearly three-fourths of the EEs surveyed report they are extremely (16%) or quite (57%) satisfied with their current positions. Yet one in four complain that they are not too (21%) or not all, (4%) satisfied." Thus, it's debatable whether the IEEE is presenting a "rosy picture" of job satisfaction.

Finally, although the Member Opinion Survey is not exhaustive on the subject of other "important issues" of job satisfaction, it does note the following: "Different age groups have different perspectives on the components of job satisfaction. Compensation is most important for those in their 50s and less important for those in their 20s and 70s. The importance of promotion increases almost linearly with age. Having authority commensurate with responsibility is least important for EEs in their 20s and most important to those in the middle- and upper-management years of the 40s to 70s. Job security is least important to those in their 70s, who are near retirement or who may already be retired. Working independently is most important for those in their 60s and least important for those in their 20s. The importance of clerical help increases with age. Continuing education is most important for the youngest engineers' job satisfaction and is least important for mid-career engineers in their 40s and 50s. Not all components of job satisfaction are age-dependent. The element rated most important for job satisfaction overall—working on interesting projects—is not significantly related to age. The same is true for having compatible colleagues, participating in decision-making about work-related issues, receiving recognition, and having comfortable workplace surroundings."

In conclusion, I appreciate your comments as an editor and as a member of the IEEE.

Sincerely yours,
Pender M McCarter
Manager, Public Information
IEEE
Washington, DC

Ed Note: EDN disagrees with Mr McCarter's statement that only EDN—and not anyone connected with the IEEE—concluded that the IEEE survey report claimed 90% job satisfaction among respondents. To quote from the IEEE report: "Just 9% say they are less than moderately satisfied."

Concerning "important issues" addressed (or not addressed) by the IEEE survey, our editorial plainly stated that the survey did *ask about*

Continued on pg 34

TEK'S COST-EFFECTIVE, 32-BIT ANSWER FOR INDEPENDENT THINKERS.

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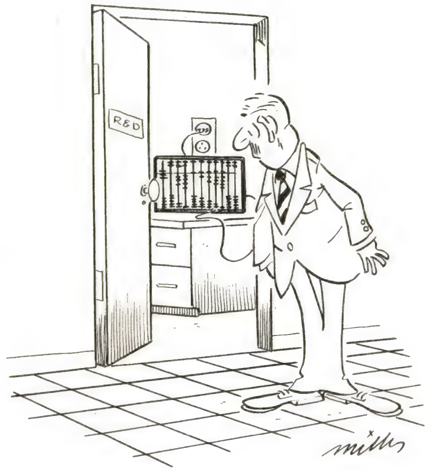
important issues. However, our editorial also plainly stated that the survey did not *ask whether IEEE members are satisfied or dissatisfied about the issues they feel are important.*

Finally, our editorial criticized only the IEEE Member Opinion Survey. We offered no criticism of the Spectrum/Harris survey, which was conducted separately.



Correction

Please note the following corrections to the Design Idea "68020 adapter upgrades 68000 systems" (EDN, January 9, pg 216). In the schematic on pg 218, IC_8 should be a 74LS191 (not an LS181) binary counter. In addition, on pg 219, the $DSACK_1^*$ line (the output of IC_{2B}, pin 3) is mislabeled. It should be named $DTACK^*$.

YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.

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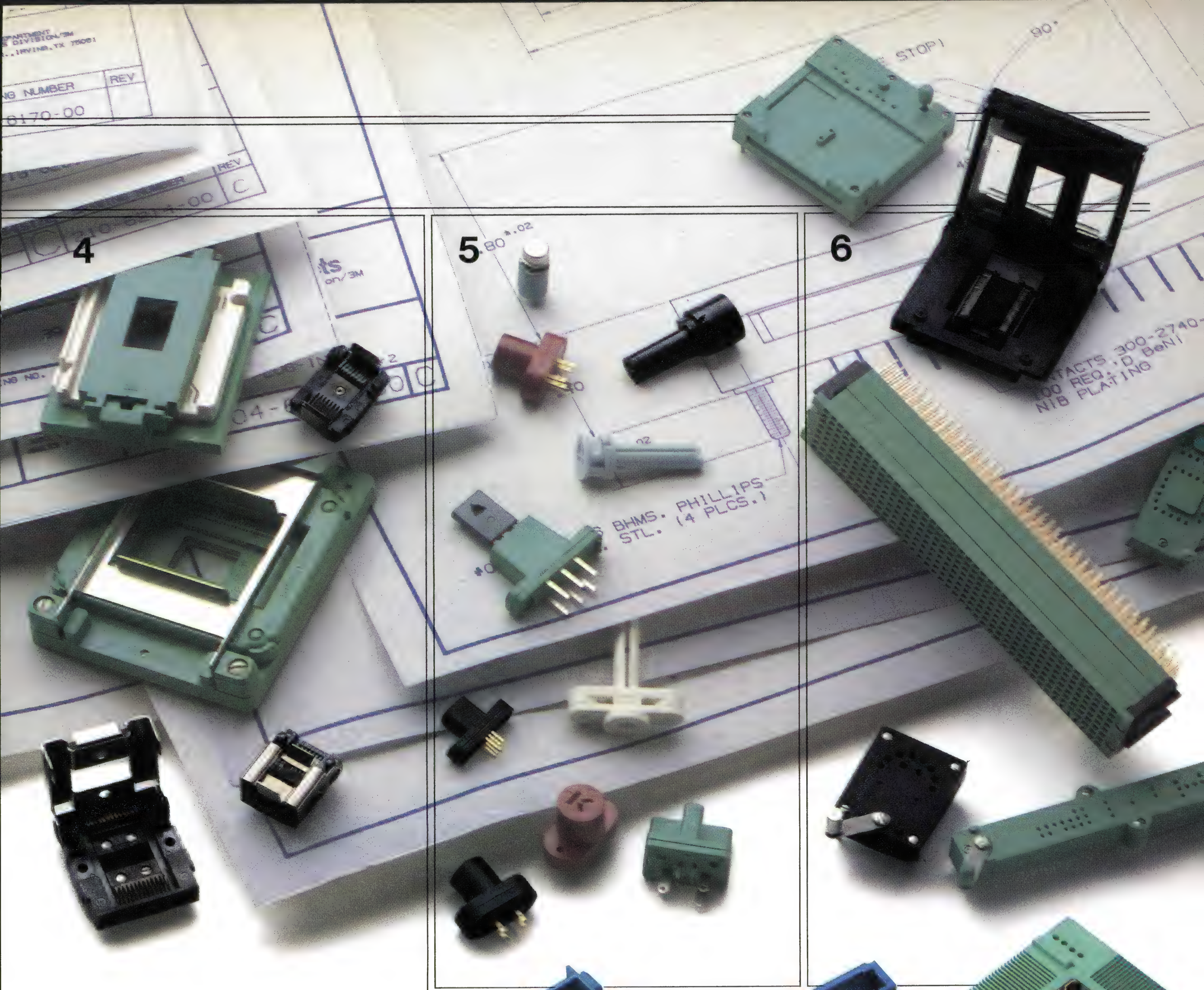
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CALENDAR

Spring National Design and Engineering Show and Conference, Chicago, IL. Banner and Greif, 110 E 42nd St, New York, NY 10017. (212) 687-7730. March 24 to 27.

IEEE Instrumentation and Measurement Technology Conference, Boulder, CO. Robert Myers, 1700 Westwood Blvd, Los Angeles, CA 90024. (213) 475-4571. March 25 to 27.

Surface Mount Technology Design Workshop, Newport Beach, CA. IPAC, Box 1869, Los Gatos, CA 95031. (408) 354-0700. March 31 to April 1.

Comdex/Winter, Los Angeles, CA. Interface Group, 300 First Ave, Needham, MA 02194. (617) 449-6600. April 1 to 3.

International Reliability Physics Symposium, Anaheim, CA. Louis DeChiaro, Registration Chairman, Box 1568, Toms River, NJ 08754. April 1 to 3.

Leadership '86 (conference on leadership, women, and high technology), Washington, DC. National Alliance for Women in Communications Industries, Box 33984, Washington, DC 20033. (202) 293-1927. April 2 to 3.

11th West Coast Computer Faire, San Francisco, CA. Computer Faire, 181 Wells Ave, Newton, MA 02159. (617) 965-8350. April 3 to 6.

Common Spring 1986 Conference (IBM Computer Users Group), New York, NY. Common, 435 N Michigan Ave, Suite 1717, Chicago, IL 60611. (312) 644-0828. April 6 to 10.

Annual Convention and Technology Exposition of the American Institute for Design and Drafting, Hollywood, FL. American Institute for Design and Drafting, 966 Hungerford Dr, Suite 10-B, Rockville, MD 20850. (301) 294-8712. April 7 to 10.

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CALENDAR

Correlation and Spectral Analysis (short course), Washington, DC. Continuing Education Institute, 10889 Wilshire Blvd, Los Angeles, CA 90024. (213) 824-9545. April 7 to 10.

IEEE Infocom, Miami Beach, FL. Steven Richman, AT&T Bell Laboratories, Room HO-3L-531, Holmdel, NJ 07733. (201) 949-1857. April 7 to 10.

Federal Office Systems Expo, Washington, DC. National Trade Productions, 2111 Eisenhower Ave, Suite 400, Alexandria, VA 22314. (800) 638-8510; in VA, (703) 683-8500. April 7 to 10.

Instrumentation '86, Portland, OR. Instrument Society of America/ Portland Section, Box 12152, Portland, OR 97212. April 8 to 10.

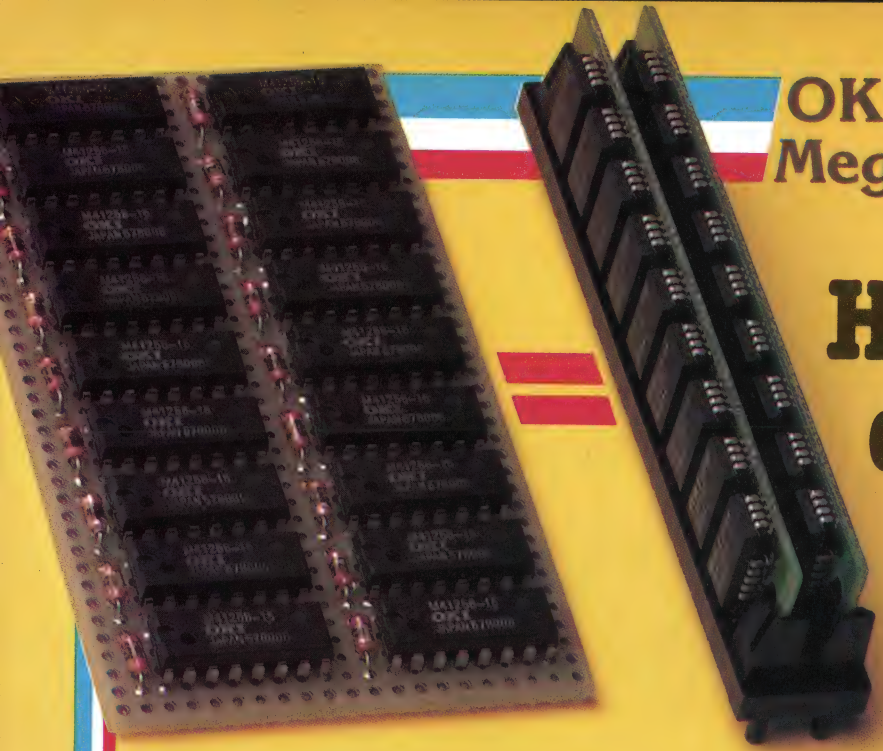
15th Annual International Programmable Controllers Conference and Exposition, Detroit, MI. Engineering Society of Detroit, 100 Farnsworth, Detroit, MI 48202. (313) 832-5400. April 8 to 10.

CommunicAsia '86 (Asian International Electronic Communication Show and Conference), Singapore. Kallman Associates, 5 Maple Court, Ridgewood, NJ 07540. (201) 652-7070. April 9 to 12.

World Market for Electronics and Electrical Engineering, Hannover, West Germany. Hannover Fairs USA, Box 7066, Princeton, NJ 08540. (609) 987-1202. April 9 to 16.

Intermag '86 (International Magnetics Conference), Phoenix, AZ. J Lemke, 2400 6th Ave, #1103, San Diego, CA 92101. (619) 755-1393. April 14 to 17.

Modern Power Conversion Design Techniques (short course), Ottawa, Ontario, Canada. E/J Bloom Associates, 115 Duran Dr, San Rafael, CA 94903. (415) 492-8443. April 14 to 18.



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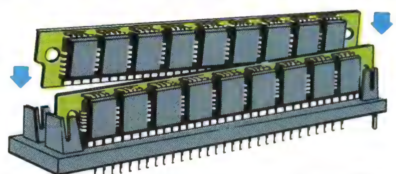

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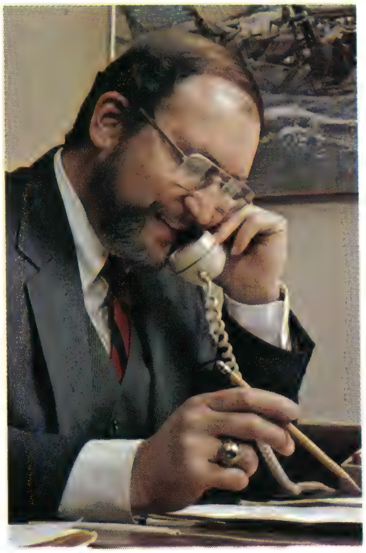

In every survey EDN has conducted that asks what kinds of editorial coverage you want, you've ranked new-product information among the top three. We use such surveys to ensure that EDN continues to help you in your job, not only by improving how we present information, but also by publishing the types of articles that you indicate you need.

Accordingly, EDN will expand its new-product coverage next month with the introduction of a tabloid-size publication called EDN *Product News*. All qualified US and Canadian subscribers will receive the publication once each month.

EDN *Product News* lets us bring you more news of product developments than we could before. *Product News* will carry in-depth feature articles on significant new products, as well as Technology Update surveys that will examine trends in different product areas. It will also give you details of the developments, products, and services of the distributors you use, along with late-breaking news of products being displayed at the major electronics shows.

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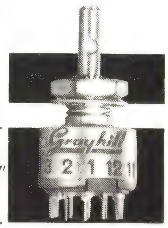

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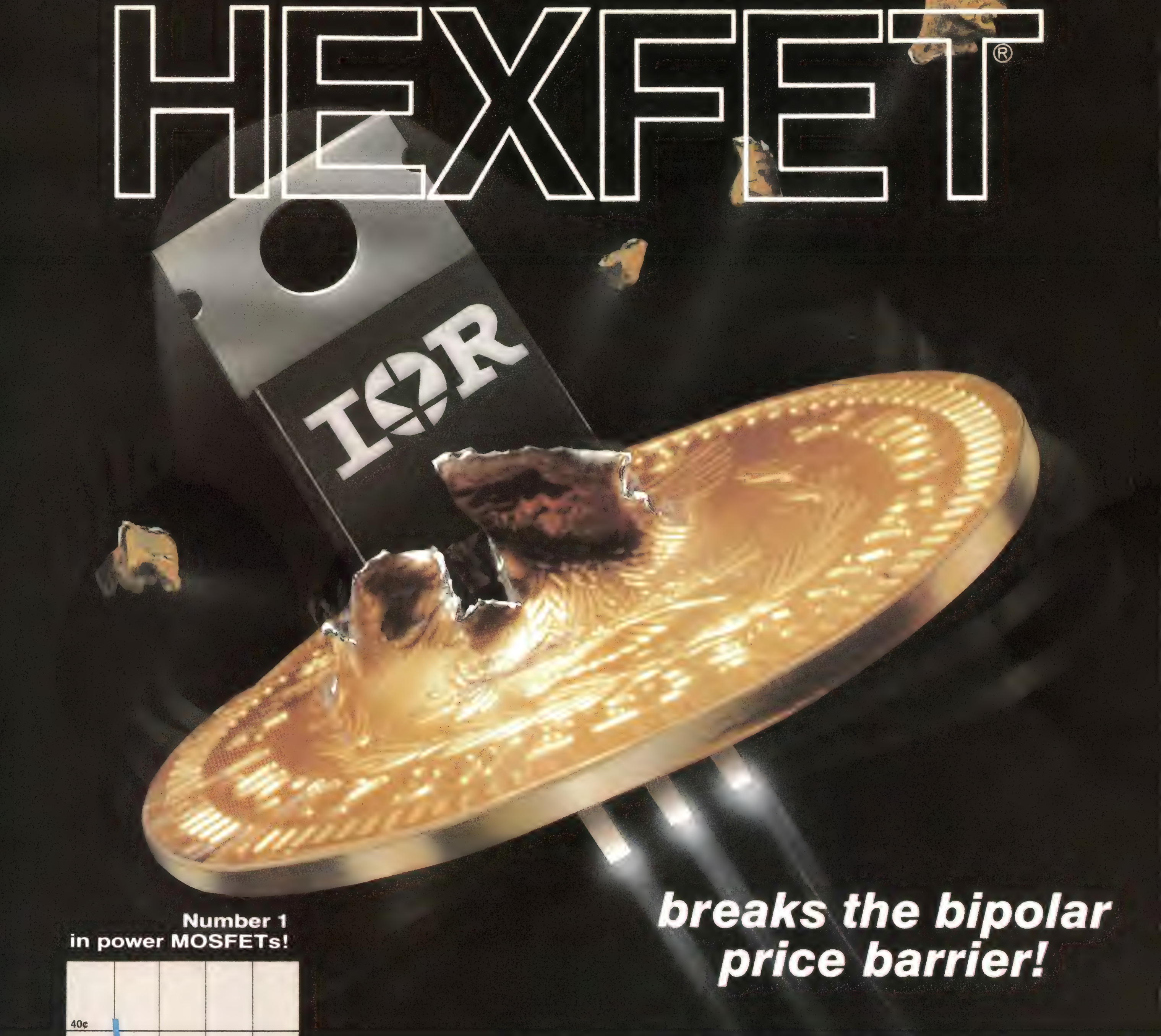

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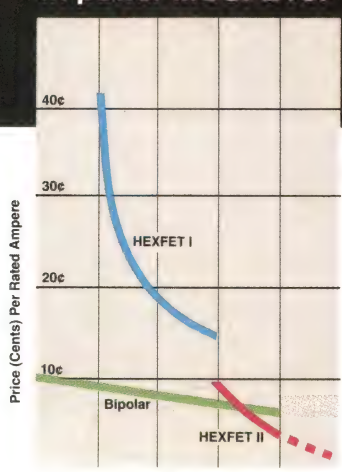

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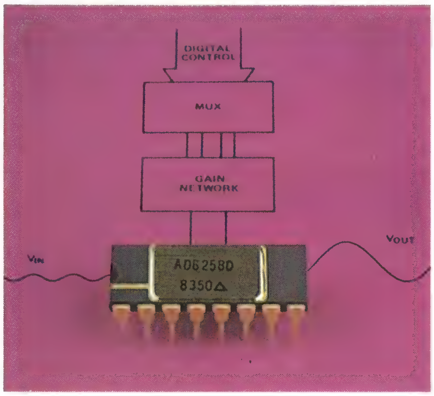
Monolithic instrumentation amplifiers save space without sacrificing performance

Tarlton Fleming,
Associate Editor

Compared with discrete designs, monolithic instrumentation amplifiers (IAs) offer closer matching and tracking of parameter values. Consequently, the ongoing refinements in circuit-design techniques and process technology have produced monolithic IAs that outperform most of the earlier hybrid, modular, and rack-mounted types. Moreover, the monolithics are frugal on board space—most come in a 14-pin DIP or TO-100 package.

Monolithic IAs employ either voltage or current feedback. Each type offers comparable performance; in fact, performance is not necessarily the key parameter in choosing between them. Proponents of each, however, generally acknowledge the subtle tradeoffs that accompany the different design approaches. Compared with voltage-feedback types, the current-feedback IAs provide inherently higher common-mode rejection without resistor matching. Yet at low gain, the current-feedback devices exhibit slightly higher gain nonlinearity and output noise, as a consequence of the design difficulties associated with their controlled active current sources.

Monolithic IAs based on the voltage-feedback arrangement are available from Analog Devices (the AD524, AD624, and AD625) and Burr-Brown (the INA101, INA102, and INA110). The first monolithic IA (the AD520 from Analog Devices), however, was based on current feedback, and this alternative is equally attractive for use in new designs. You can buy the current-feedback type of IA from Precision

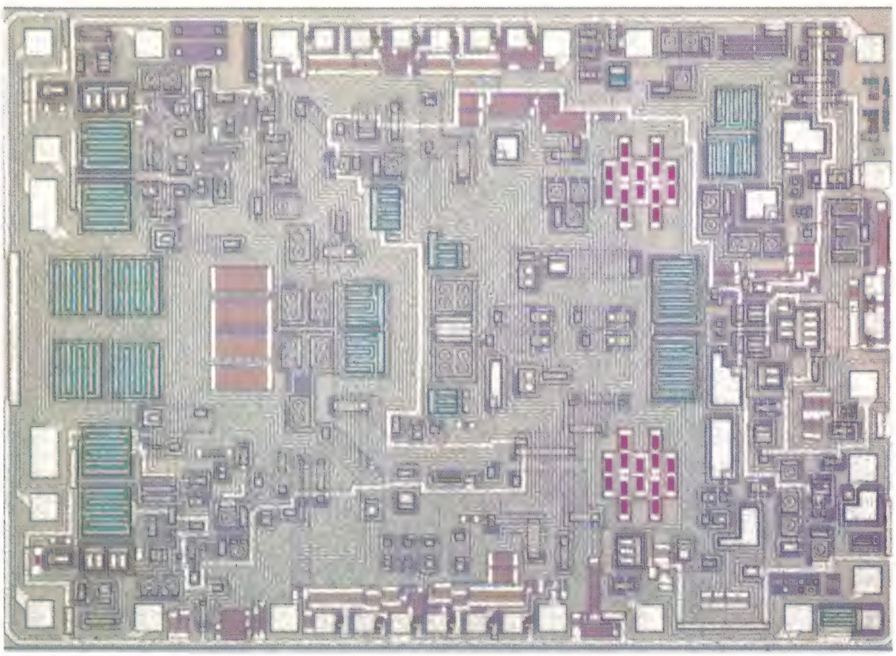


For use in software-programmable gain applications, *the monolithic AD625 from Analog Devices is a voltage-feedback type of instrumentation amplifier.*

Monolithics (the AMP-01 and AMP-05), National Semiconductor (LM163), and Analog Devices (AD521).

Non-monolithic IAs are usually based on a traditional voltage-feedback design that includes three op amps and a resistor network **(Fig 1)**. Today, these older products serve primarily as replacements in established systems. Moreover, because the rack-mounted IAs (such as Preston Scientific's DX-A2) often include active filters, a line-operated power supply, and other functions in addition to the IA, they are better regarded as instruments rather than IAs. By today's standards, these amplifiers are unreasonably large and heavy for what they do.

If your application demands better performance than commercially available monolithic IAs can provide, consider building your own IA. You can accomplish this task by combining a resistor network with one, two, or three op amps according to the performance level you require (see **box,** "Building blocks for IAs"). Further, an unusually low-noise or high-bandwidth requirement may compel you to build



A JFET-input device, *the AMP-05 from Precision Monolithics, specs 12-μsec max settling at a gain of 1000.*

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CIRCLE NO 95

an IA using matched dual transistors in addition to special-purpose op amps and the resistor network (**Ref 1**). Note that the instrumentation op amps offered by some manufacturers are suitable for use in building an IA, but they are not IAs by themselves.

Regardless of design details, IAs generally provide precise, differential voltage amplification, high input impedance, and a high level of common-mode voltage rejection. You probably need an IA (rather than a conventional op-amp circuit) if your signal requires differential amplification; if the signal is also mixed with unwanted noise and common-mode voltage, an IA is required. (On the other hand, if the sum of signal, noise, and common-mode voltage exceeds the IA's input range, you may need an isolation amplifier—a more specialized device.)

To enhance their precision signal-handling capabilities, most IAs provide output-sense and reference terminals, and some provide a guard-drive terminal as well. The sense terminal helps the IA develop an accurate voltage across a remote load; otherwise you connect the sense terminal to V_{OUT} at the amplifier. Connecting sense directly to a remote load, however, excludes the line drop caused by load current flowing from the amplifier to the load. Similarly, the reference terminal can exclude line drop caused by load current flowing in the ground path. Also, the reference input allows you to introduce a large and deliberate output offset, or to accommodate input and load signals having different return potentials.

The guard-drive terminal, provided with some IAs, is a common-mode voltage derived from the input signal and made available as a low-impedance source for driving the input signal's cable shield. Maintaining the signal conductor and shield at the same common-mode voltages aids rejection of these voltages by reducing their differential phase shift at the IA inputs.

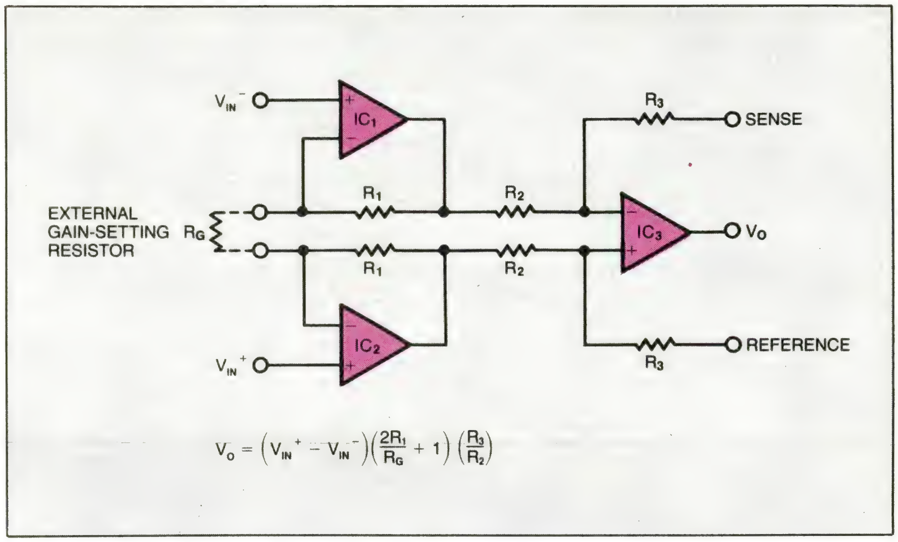


Fig 1—Most instrumentation-amplifier designs *are based on this basic 3-op-amp arrangement and variations on it. Gain is determined by external resistor R_G.*

Building blocks for IAs

For applications that require better performance than off-the-shelf IAs can provide, you can use several products to construct your own. You can also use IAs as building blocks for higher-level assemblies (see **box,** "IAs as system components").

The IA's critical front-end stage, for example, may require discrete, dual matched-transistor ICs to achieve unusually low noise or low offset-voltage drift requirements. These matched transistors are available from such manufacturers as Micro Power Systems and Precision Monolithics.

As another approach in building your own front-end stage, consider Linear Technology's LTC1043CN, a monolithic CMOS device that uses switched-capacitor technology to provide a dual front end for IAs. In addition, the \$2.95 (100) part can implement differential to single-ended signal conversion, voltage inversion, and voltage multiplication and division.

The INA105 unity-gain differential amplifier from Burr-Brown is another building-block IC for IAs. Offering 0.001% gain nonlinearity and −86-dB common-mode rejection, the INA105 can serve as the output subtractor stage in a conventional 3-op-amp IA. It also allows various other precision-gain connections to be made, including a 4- to 20-mA current transmitter. The INA105, in a plastic miniature DIP, costs \$3.50 (100).

Adaptive gain changing

As an additional feature, most IAs include provision for changing their voltage gain so they can accept signals spanning a wide dynamic range. Most let you make fixed-increment changes in gain, either by jumper-selection of internal resistors or by changing external resistors. In either case, you can select gain via software by adding an external multiplexer.

To avoid unnecessary engineering, however, you can choose a ready-made hybrid IA that includes gain-select circuitry along with la-

ser-trimmed thin-film gain resistors. (Most programmable-gain IAs are found in larger subassemblies—hybrid, modular, and board-level data-acquisition systems.)

Burr-Brown's PGA200/201, for example, a voltage-feedback IA, provides gains of 1, 10, 100, or 1000 (or 1, 8, 64, or 512 in the 201 version) in response to a 2-bit TTL-compatible digital input. The same 2-bit control words enable National Semiconductor's LH0084 to provide gains from 1 to 100 (1, 2, 5, or 10 in the input stage, multiplied by a pin-strappable gain of 1, 4, or 10 in the output stage). **Table 1** provides other performance parameters and pricing information.

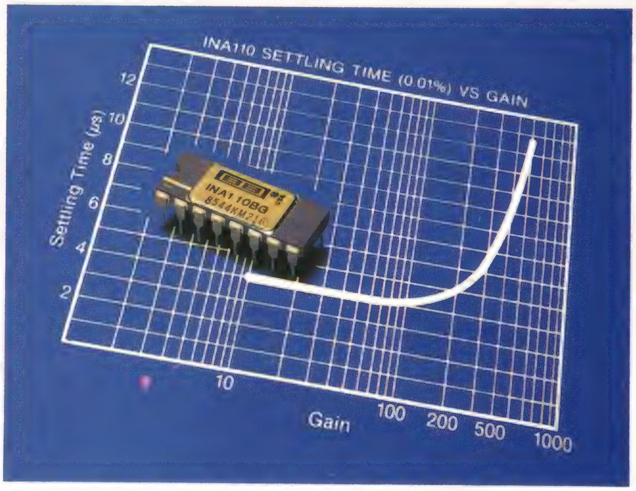
Analog Devices' AD524 and AD624 voltage-feedback IAs also include the gain-setting resistors on chip, and they allow you to arrange for software-programmable gain by adding external gain-select switches. The resulting gain accuracy is limited by the external switch on-resistance, however, which falls in series with the internal precision-trimmed resistors.

IAs as system components

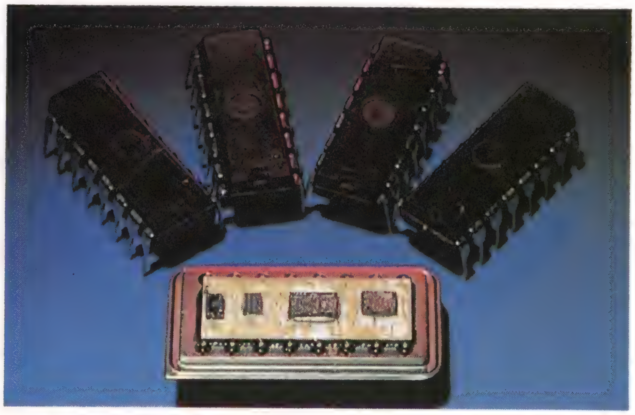
In addition to stand-alone products, 1-chip IAs serve as components in higher-level assemblies. The $61 (100) AD365 from Analog Devices, for example, combines the AD625 IA and AD585 track/hold amplifier with a multiplexer and thin-film resistor network. The resulting hybrid provides software-programmable gain and track/hold functions in a 16-pin DIP—suitable for use as the front end of a data-acquisition system.

Designed for noisy industrial environments, Burr-Brown's monolithic XTR101 4- to 20-mA, 2-wire transmitter includes a 2-op-amp IA among other functions on the chip. The $7.45 (100) product transmits its signal and receives power over the same pair of wires, while providing a maximum 30-μV offset voltage and 0.01% nonlinearity error.

In addition, board-level data-acquisition systems often feature a programmable-gain IA to buffer the analog-multiplexer output, although an IA in each channel preceding the multiplexer offers more advantages: a higher rate of channel switching, plus the option of including signal filtering without a throughput penalty. The $1995 DT5732 from Data Translation is such a product. It includes four differential channels with an IA in each, a multiplexer, sample/hold circuitry, and a high-speed 12-bit A/D converter. Throughput is 800,000 samples per second.



High-speed settling is an advantage *of the JFET-input INA110 instrumentation amplifier from Burr-Brown.*



Offering digitally controlled gain *and a track/hold function, the hybrid AD365 from Analog Devices includes a monolithic instrumentation amplifier (the AD625) as a component.*

When used to buffer the multiplexer in a data-acquisition system, the IA often constitutes a speed bottleneck, especially at high gain. Burr-Brown's INA110 and Precision Monolithics' AMP-05 monolithic IAs address this problem. Both bipolar devices use JFET inputs for speed as well as for low input bias current. Maximum settling times are 5 μsec to 0.01% at a gain of 500 for the INA110 and 12 μsec to 0.025% at a gain of 1000 for the AMP-05.

The INA110 is a 3-op-amp voltage-feedback type that includes a thin-film resistor network providing pin-strappable gains of 1, 10, 100, 200, and 500. The AMP-05 current-feedback type allows you to set any gain from 0.1 to 2000 by adding two external resistors. It also includes dual guard drivers to reduce the effects of input cable capacitance and an uncommitted 100-μA current source for exciting transducers or powering a low-current voltage reference.

11-Bit Flash Converter

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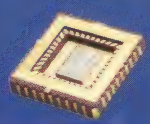

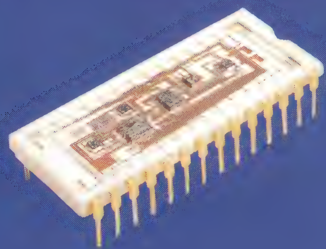

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The problem of limited gain accuracy is eliminated in the company's AD625 software-programmable-gain IA. Although you must supply an external gain-select multiplexer and the external gain-setting resistors, this device offers high accuracy (5-ppm/°C gain TC max and 0.001% gain nonlinearity for a gain of 1) and an architecture suited to custom gain arrangements from 1 to 10,000. The external switches don't affect gain accuracy because their on-resistance connects directly to the IA's high-impedance inputs.

IAs include preamp stage

The monolithic AD524, AD624, and AD625 IAs come in 16-pin DIPs and share the same circuit architecture—a modification of the standard 3-op-amp IA design. Each includes an input preamplifier stage whose transconductance increases with programmed gain, yielding a gain-bandwidth product of 25 MHz at a gain of 1000. This adaptable-gain preamp stage also reduces gain nonlinearity by boosting the loop gain available at higher programmed

TABLE 1—REPRESENTATIVE INSTRUMENTATION AMPLIFIERS

MANUFACTURER AND MODEL	GAIN NONLINEARITY ERROR (G=1000) (% OF FS MAX)	COMMON-MODE REJECTION (G=1) (dB MIN)	NOISE, RTI		INPUT BIAS CURRENT (nA MAX)	INPUT OFFSET VOLTAGE (G=1) (μV MAX)	−3-dB BANDWIDTH (G=1000) (kHz TYP)	SETTLING TIME (±0.01%, G=1000) (μSEC TYP)	PRICE (100) ($)	COMMENTS
			(0.1 TO 10 Hz, G=1) (μV p-p TYP)	DENSITY (f=1 kHz, G=1000) (nV/$\sqrt{Hz}$ TYP)						
ANALOG DEVICES AD521KD	0.2	74	225 (RTO)	—	40	1500	40	35	16.40	
AD522BD	0.005	80	—	—	25	200	0.3	—	39.00	HYBRID
AD524CD	0.01	80	15	7	15	50	25	75	17.95	
AD624CD	0.005	80	10	4	15	25	25	75	23.35	
AD625CD	0.005	80	10	4	15	25	25	75	22.50	
BURR-BROWN INA101CG	0.025	80	0.8	13	20	450	2.5	350	16.35	
INA102CG	0.05	80	0.1	25	30 (T_{MIN} – T_{MAX})	300	0.3	4500	11.35	LOW POWER
INA110	0.02 (G=500)	80	8	10 (10 kHZ)	0.05	3250	100 (G=500)	16 (G=500)	12.35	JFET INPUTS
PGA200BG	0.012	80	0.8	13	20	225	2.4	670	41.00	DIGITALLY PROGRAMMABLE
INTERSIL ICL7605	—	100 (TYP)	4	—	1.5	5	0.01	—	11.80	LOW BW; AUTO-ZEROED
NATIONAL SEMICONDUCTOR LM363D	0.03	88 (G=10)	10 (G=10)	12	10	100 (G=10 TYP)	—	70 (0.1%)	15.00	
PRECISION MONOLITHICS AMP-0IEX	0.005	90	13	5	3.0	50	26	50	16.90	
AMP-05EX	0.02 (TYP)	90	—	16	0.05	—	120	10 (0.025%)	19.90	JFET INPUTS
PRESTON SCIENTIFIC DX-A2	0.005	100 (G=10)	0.2	—	1.0	5	40	50 (0.1%)	570.00 (1-9)	RACK-MOUNTED
TELEDYNE PHILBRICK 4253	0.01	76	—	—	−0.01	1000	5	250 (0.1%)	178.00	JFET INPUTS; MODULE

NOTES:
PARAMETER VALUES ARE AT 25°C UNLESS OTHERWISE SPECIFIED.
BW BANDWIDTH
FS FULL SCALE
G GAIN
RTI REFERRED TO INPUT
RTO REFERRED TO OUTPUT

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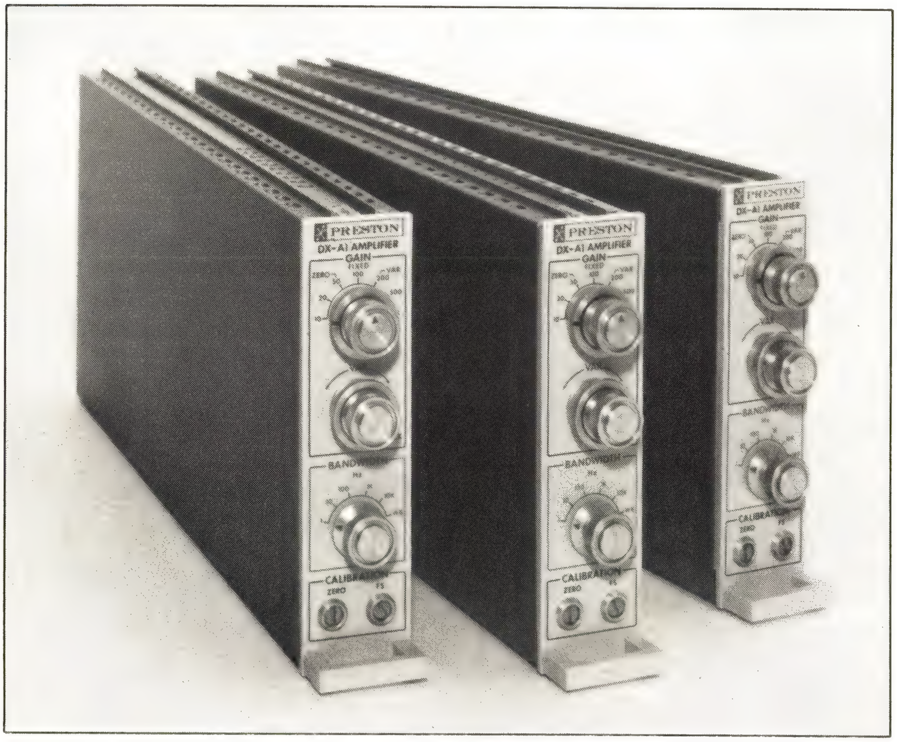

Series DX rack-mounted instrumentation amplifiers *from Preston Scientific include fixed and variable gain controls, a bandwidth-selection switch, and adjustments for full-scale and zero output.*

gains, and suppresses noise (to 4 $nV/\sqrt{Hz}$ referred to input (RTI) at 1 kHz with a gain of 500).

Three op amps form classic IA

Burr-Brown also provides several monolithic IAs based on the classic 3-op-amp voltage-feedback design. The INA101 (available also from Micro Power Systems) includes all but one of the necessary gain-setting resistors in a laser-trimmed thin-film network. You set the gain as required by supplying the missing resistor externally. A related product, the 3-op-amp INA102, offers low power consumption (750-μA quiescent current with ±15V supplies.) It also includes all resistors necessary for gains of 1, 10, 100, and 1000, selected by an external pin jumper. Packaged in a 16-pin DIP, the INA102 provides access to both inputs of the output amplifier, so you can create a balanced filter by adding external capacitors.

Teledyne Philbrick's Model 4253 is another voltage-feedback 3-op-amp IA, featuring hybrid construction and FET inputs for low input bias current (−10 pA max at 25°C). You add an external resistor to set any gain between 1 and 10,000. This IA also includes a fourth op amp to buffer the output reference terminal, thereby removing an application problem common to this type of IA: Without the buffer, any parasitic resistance between the reference terminal and system ground (as found in a pc trace, for example) degrades common-mode rejection by upsetting the match between internal resistors.

An alternative design technique

In contrast to the voltage-feedback type of IA, Precision Monolithics' AMP-01 embodies the current-feedback approach for standard-product monolithic IAs **(Fig 2).** You set the gain by connecting two external resistors, R_{GAIN} and R_{SCALE}. Active linear current sources then constrain the flow of internal signal currents so that V_{IN} is impressed across R_{GAIN}, creating a current V_{IN}/R_{GAIN}. This current is forced to flow through R_{SCALE}, producing a voltage proportional to V_{OUT}. Consequently, $V_{OUT}/V_{IN}=20\times R_{SCALE}/R_{GAIN}$. (The gain factor of 20 is produced by the 20:1 resistive dividers R_1/R_2 and R_3/R_4.)

The AMP-01 achieves low input bias currents (1 nA typ at 25°C) through a combination of superbeta input transistors and a bias-current-cancellation scheme. Furthermore, the AMP-01's output stage is stable with a 1-μF load capacitance, and the part delivers ±50 mA at ±10V. This output capability is unique

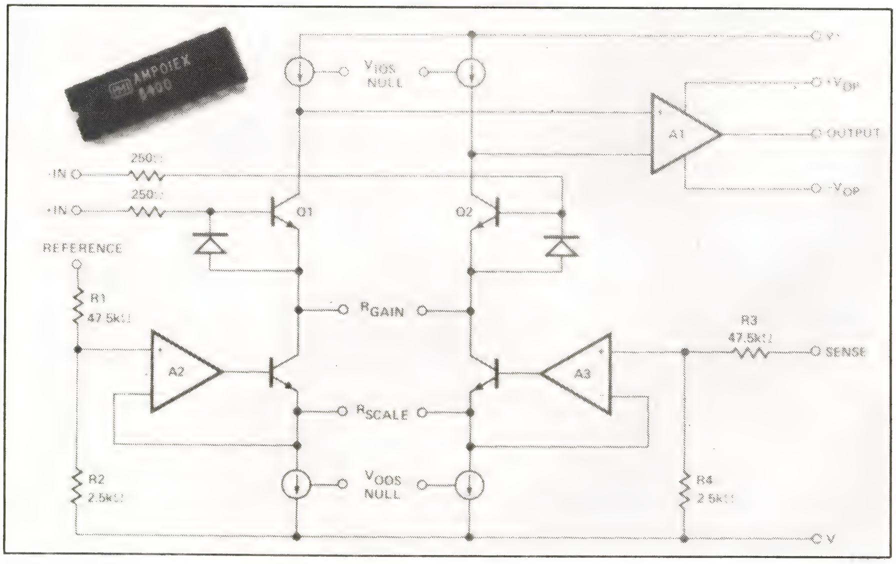

Fig 2—Using current-feedback techniques, *the AMP-01 from Precision Monolithics is a 1-chip instrumentation amplifier.*

among monolithic IAs. Although it burdens the IC with power dissipation, it also lets you drive coaxial cables directly, eliminating the current-buffer stage required with less robust IAs.

IA uses thin-film resistors

Another monolithic current-feedback IA, the LM363 from National Semiconductor, includes on-chip thin-film resistors for jumper-selectable gains of 10, 100, or 1000 for the 16-pin DIP version. You can obtain other gain values (greater than 10) by adding external resistors. The LM363 provides sense and reference terminals plus twin differential guard-drive outputs, which you can connect to the shields of separate input-signal cables to reduce bandwidth loss.

Finally, the ICL7605, which manufacturer Intersil calls a commutating autozero instrumentation amplifier, demonstrates a novel approach in realizing the IA function. Suitable only for low-frequency signals (dc to 10 Hz), this monolithic CMOS device first converts the differential input to a single-ended signal using flying capacitors and analog switches. Next, two CMOS op amps provide autozeroing and amplification by alternating these duties at approximately 160 Hz. As a result of this continuous automatic correction of internal errors, the IA offers a 2-μV offset voltage with 0.2 μV/year and 0.05 μV/°C of drift. You supply six external components: two resistors to set the gain (1 to 1000), two input capacitors, and two autozero capacitors. **EDN**

Reference

1. Cate, Thomas M, "Instrumentation Amplifiers, Design and Application," Wescon/85, Session 36, San Francisco, CA, November 1985.

Article Interest Quotient
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For more information . . .

For more information on the instrumentation amplifiers described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

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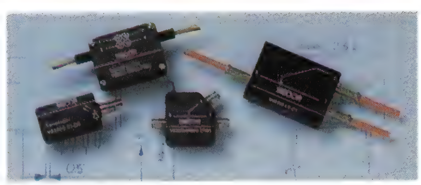

Left to right: 200 MBaud transmitter, fiber optic switch, WDM, T-coupler with pigtail.

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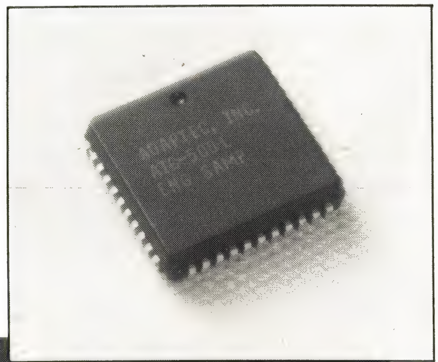
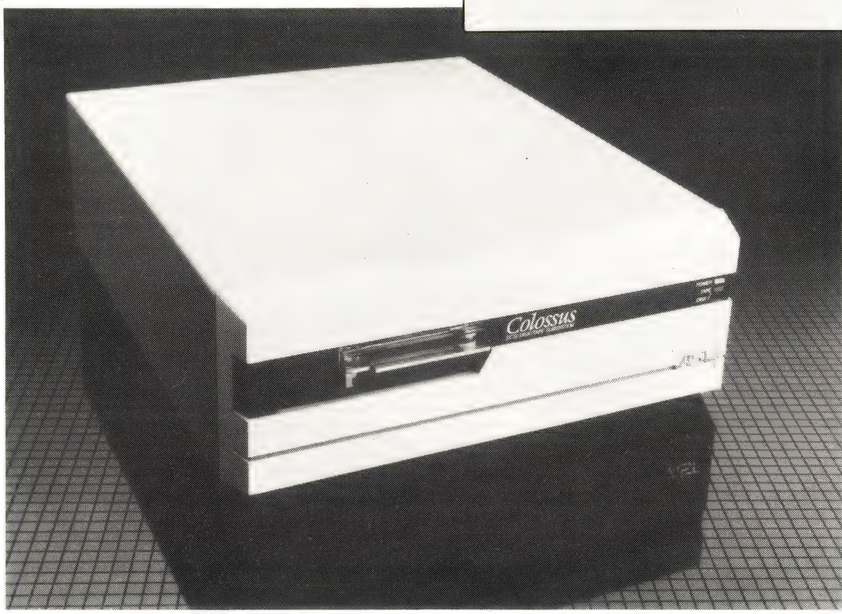
Improved throughput vies with flexibility in disk-controller interface standards

Chris Terry, *Associate Editor*

Flexibility is a goal in many computer-system designs, and high data throughput is desirable in most. But when it comes to selecting disk controllers, you must tolerate some tradeoff between these virtues. For high throughput, a dedicated, high-speed drive works best with a drive-level controller that's tightly coupled to the system interface. If you want flexibility—in terms of connecting drives and other peripherals from various manufacturers, or in terms of allowing two hosts to share the same resources—an intelligent disk controller is preferable.



One of a family of disk-controller chips, *this VLSI device from Adaptec implements the full SCSI scheme.*



Allowing easy expansion of storage facilities *by connecting extra drives to the SCSI bus, the Colossus disk subsystem works with IBM PC/XTs and PC/ATs.*

The increasing demand for improved data-transfer rates is a result of technological developments. Advances in hard-disk-drive head technology, new encoding techniques that yield greater bit densities on each track, and the increasing use of VLSI multifunction controller ICs have combined to make possible the storage of as many as 380M bytes on a 5¼-in. drive and 600M bytes or more on an 8-in. drive. For a given disk-rotation speed, an increase in bit density requires a corresponding increase in data-transfer rate. The system designer who wishes to exploit the full capabilities of the new drives must therefore consider not only the problems of keeping track of large amounts of data, but also the question of which CPU/disk interface will support the required data rate.

Interest in new interfaces

The two de facto drive-interface standards—the Seagate ST506 at the low end (ie, microcomputers), and the Storage Module Drive (SMD) interface at the high end (ie, mainframes)—are both proving inadequate, largely because neither can support the high data-transfer rates now in demand. The Shugart Associates System Interface (SASI) and its successor, the Seagate ST506/412 interface, handle maximum data-transfer rates of 5M bps (625k bytes/sec). The SMD interface originally specified an upper limit of 10M bps (1.25M bytes/sec) and, even more inconveniently, a maximum of 20,160 bytes per track. The latter limitation precludes any substantial increase in the storage capacity of an SMD drive. In addition, the SMD interface, like any drive-level interface, requires that the host CPU assume the burden of translating logical block numbers into physical track and sector numbers.

Consequently, for systems requiring high data-transfer rates, there is a growing interest in two interfaces: the 2.5M-byte/sec Enhanced Small Device Interface (ESDI), a drive-level interface for supermicros and minicomputers, and the 10M-byte/sec Intelligent Peripheral Interface (IPI) for superminis, mainframes, and supercomputers. The IPI, which in all likelihood will supersede the SMD interface, has the additional advantage of providing device-independent data-

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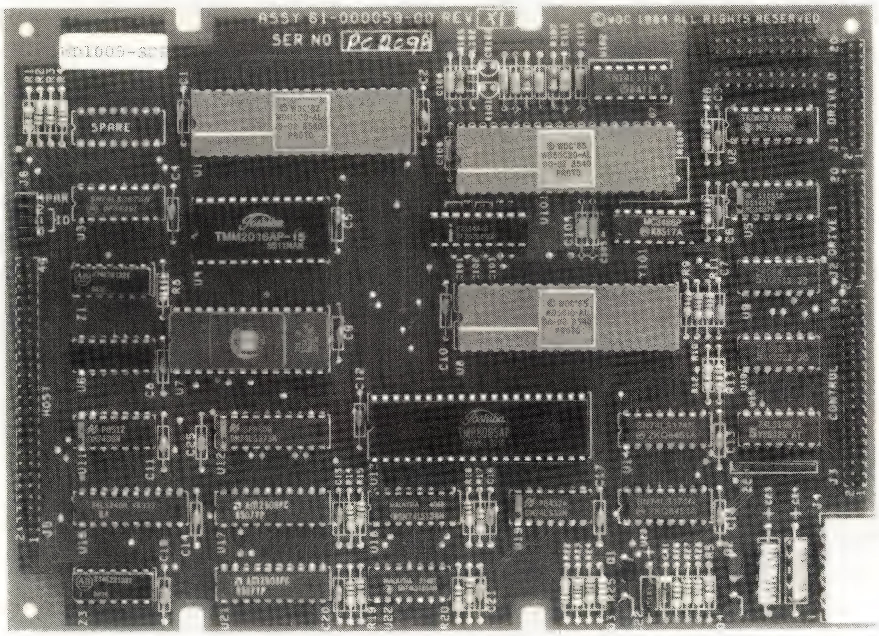
management capabilities.

There is little doubt that the Seagate ST506/412 interface is adequate to the task of providing the data-transfer rates required by microcomputer systems. Even so, schemes mandating the use of intelligent disk controllers (IDCs) are gaining in popularity at this level. In particular, the 2.5M-byte/sec Small Computer System Interface (SCSI) for microcomputer systems is attracting a great deal of attention. The SCSI's maximum data-transfer rate is not regarded as a serious drawback in such systems, while its flexibility is a definite plus.



Providing a host interface with all the features of the SCSI bus, *the WD1005-SCS from Western Digital lets you connect as many as four 150M-byte drives.*

Midrange mystification

At present, the choice of a disk interface for middle-range systems—supermicros, minicomputers, and superminicomputers—is less clear-cut. By some accounts, you sacrifice more than just throughput by leaning toward SCSI-style flexibility at this level. In this range, many computer manufacturers are migrating to the VME Bus or Multibus II, both of which have a maximum data-transfer rate of 3M to 4M bytes/sec. The problem facing disk controller manufacturers is how best to match an available drive interface to the capabilities of a high-performance computer bus. Software considerations influence the solution to some degree, particularly if you're upgrading an existing system.

Xylogics takes the view that any scheme requiring a host adapter (for example, the SASI or SCSI schemes) and intelligent disk controllers merely interposes an intermediate bus between the CPU and the formatter portion of the controller, thereby reducing efficiency and possibly creating more problems. The Xylogics solution is to provide a standard VME or Multibus interface to the host and a storage-management and data-transfer controller that's tightly coupled to a formatter on the same board.

To avoid potential conflicts between disk and tape commands, some Xylogics boards incorporate a separate tape-drive controller. The Xylogics 422, for example, is a Multibus board that incorporates both ESDI disk and QIC-02 tape controllers. You load a disk or tape command into an I/O parameter block (IOPB) and initiate the command by passing the IOPB address to the controller. You can chain IOPBs so that the controller can execute complex sequences of both disk and tape commands with little or no host involvement.

Xylogics offers VME and Multibus I controllers with an ESDI or an enhanced SMD disk interface for high-performance systems, and an ST506 interface for systems with less-stringent requirements. A line of Multibus II controllers is in the development stage.

Other controller manufacturers for middle-range systems appear to be following the Xylogics example. Dual Systems offers a VME Bus disk controller that controls as many as four ESDI drives with data-transfer rates as high as 20M bps. The controller's 250k-byte cache memory has parity-error detection and uses an algorithm that, the company says, improves file-system read operations under the Unix operating system. DMA data transfers to and from the host can be in 16- or 32-bit format (software selectable) at rates as high as 1.2M bytes/sec.

Intelligence for interrogation

Despite the caveats, the demand for intelligent controllers and host adapters is increasing, according to Joseph Jaworski, president of Peripheral Concepts, an Irvine, CA, market-research organization. Controller manufacturers, he says, generally agree that you achieve the best performance (in terms of speed) from a device-level formatter that's tightly coupled to the system interface. However, a full implementation of the SCSI allows the host to interrogate a peripheral regarding its capacity, data-transfer rate, and other characteristics, and to adjust to these conditions under program control instead of manually resetting DIP switches or jumpers.

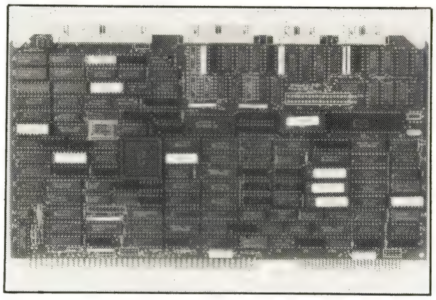
Jaworski points out that this feature makes the SCSI very attractive to a system integrator whose

principal concern is to provide for easy field upgrades of the system, and who can tolerate the slight loss in efficiency entailed. For that reason, Jaworski believes that the VME Bus market, growing rapidly but currently fragmented among many suppliers of board-level products, will contribute to the growth of SCSI controllers, and that growth of the market for VME Bus host adapters will exceed 85% from 1985 through 1987.

It's clear that interest in the SCSI is accelerating. In October of 1985, more than 50 companies attended a SCSI forum held in the Boston area, and nearly every disk-controller manufacturer now offers SCSI products or is in the process of developing them. A further indication of the general interest in this interface is the fact that Apple incorporated a SCSI port into the Mac Plus computer. What's more, in spite of the tendency to regard the SCSI as a slow interface for low- and middle-range systems, experiments at Adaptec indicate that use of the synchronous mode can yield data-transfer rates as high as 5M bytes/sec.

"SCSI" spells flexibility

The word "small" in the SCSI name is intended only as a relative characterization: The SCSI bus can handle the I/O functions of quite complex systems containing not only disk drives, but also tape drives, printers, network gateways, and other peripherals. One SCSI controller, now available as a single VLSI chip from Adaptec, Ferranti, Fujitsu, and other sources, can control as many as eight peripherals, and a system may have more than one SCSI controller. The devices on the bus may be either initiators or targets. If there is more than one initiator, you must implement the arbitration facilities of the standard. A single-initiator, multitarget configuration implies that a single host computer is controlling a variety of peripherals; a multiple-initiator configuration implies that peripheral resources are being shared between two or more host computers.



***This controller board for the VME Bus,** the Xylogics 422, incorporates the ESDI for connection to disks, a QIC-02 tape interface, and a controller that can perform complex commands without host involvement.*

The SCSI bus and handshaking protocols are defined in the proposed ANSI standard X3T9.3. Because there are currently five groups of commands (one basic and two extended command sets for data transfer, status, and control, and two groups for vendor-unique commands), full exploitation of the capabilities is not a simple matter. Nevertheless, most disk-controller vendors and drive manufacturers either have SCSI products available now or plan to introduce them. Adaptec, for example, has just added a SCSI chip to its I/O-controller chip set. The company also provides a SCSI interface on its disk-controller boards, which through use of 2,7 RLL encoding can expand the capacity of Seagate, Rodime, and similar drives by 50%. In other words, a drive that would store 20M bytes with modified-FM encoding can store 30M bytes when attached to an Adaptec controller board.

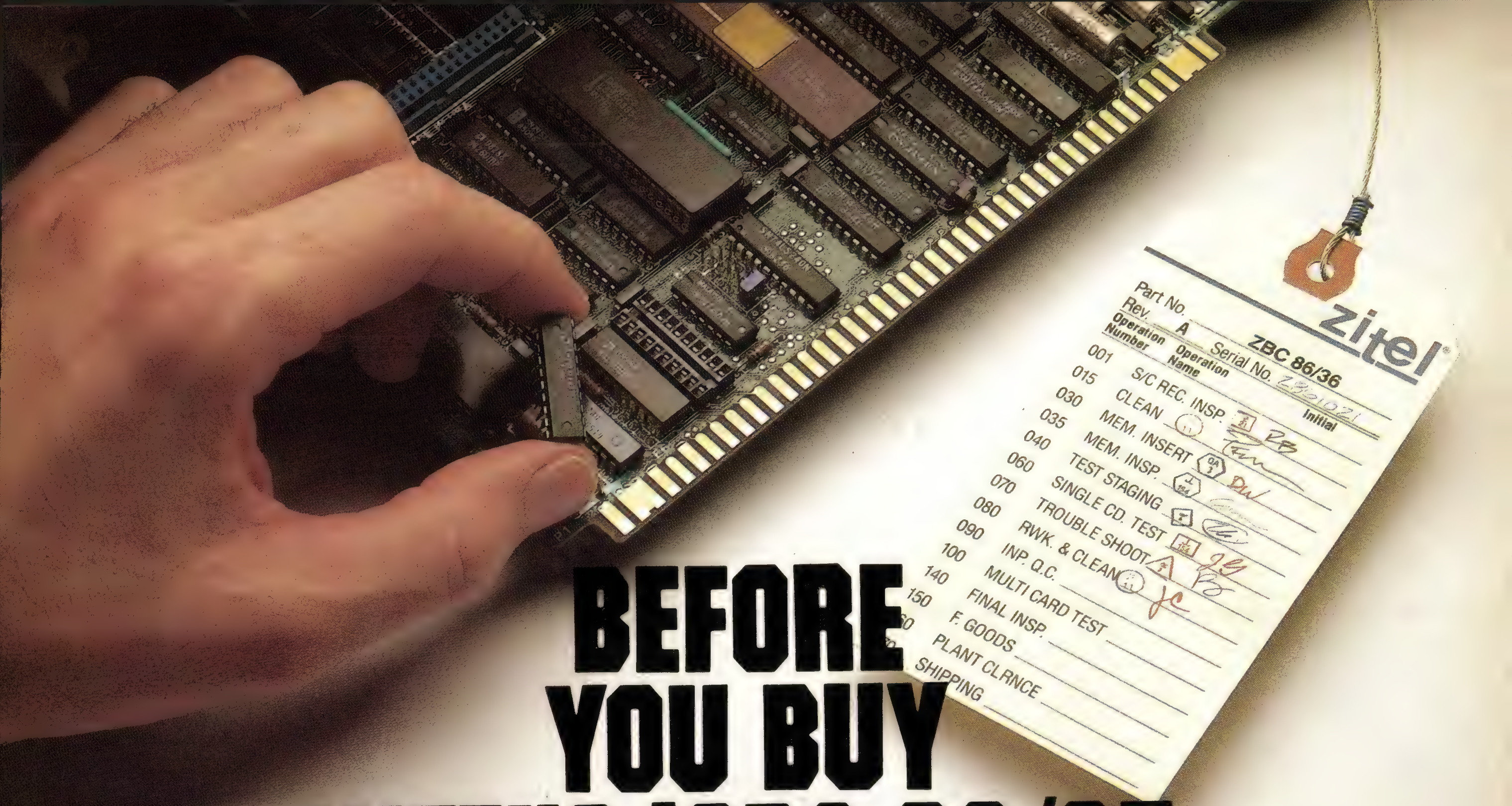
The SCSI bus also facilitates relatively easy expansion of storage capacity. AST Research recently introduced the Colossus 74M-byte disk subsystem for IBM PC/XTs and PC/ATs. The Colossus subsystem includes a 60M-byte tape-cartridge drive for backup. You can expand the total storage capacity to 370M bytes by connecting additional drives to the SCSI bus, which is integrated into the disk subsystem, so you don't need any additional slots in the PC for the expansion.

You can take advantage of SCSI facilities to select drives from several different manufacturers and either mix them in the same system or designate one vendor as your primary source and the others as secondary sources of replacement drives. You can do so because a number of controller manufacturers are now using the SCSI as their standard interface to the host computer and an ST506/412 interface, ESDI, or SMD interface as the drive connection.

The Adaptec ACB 5500 controller board, for example, uses the SCSI on the host side and the ST506/412 interface on the drive side. Another board from the company, the ACB 5580, uses the SCSI and the SMD interface. Emulex offers the MD21 controller, which interfaces any two large-capacity, serial-mode ESDI 5¼-in. drives to the SCSI bus. The company also offers SCSI host adapters for DEC Q Bus and Unibus systems, Multibus systems, and IBM PCs, PC/XTs, and PC/ATs and compatible systems.

Fujitsu also recently introduced a SCSI-based intelligent disk controller (IDC). The M1054X IDC handles as many as four Fujitsu M2246E 5¼-in. drives to yield a total formatted capacity of 600M bytes. The IDC incorporates an ESDI drive interface to yield a data-transfer rate of 1.25M bytes/sec between the controller and the drive. The interface between the IDC and the host is the 8-bit-parallel SCSI, with a data-transfer rate of 1.5M bytes/sec in synchronous mode. The M1054X IDC can operate with the new Common Command set of the SCSI protocol, but it also operates with an enriched command set.

Scientific Micro Systems offers the OMTI Series 7000 multifunction SCSI controllers, and the company recently introduced the OMTI 7100 IDC. This controller operates with ST506/412 drives as well as with soft- and hard-sectored ESDI



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drives. It detects and segregates defective sectors and provides a list of recorded defects. The host interface is a multiple-initiator, multitarget implementation of the SCSI that provides bus arbitration, multithreaded operations, message-system support with disconnect/reconnect, and 1:1 interleave operations. The IDC can operate with the Common Command set as well as all SCSI command sets.

Western Digital is another company that offers controllers with a SCSI connection to the host. The WD1003A-SC IDC handles a choice of one or two ST506/412 disk drives, and the WD1005-SCS IDC can handle as many as four ESDI drives. Both IDCs act as target devices in the SCSI environment and provide all SCSI features, including arbitration, disconnect/reconnect operations, and synchronous data transfers at rates as high as 1.5M bytes/sec. The boards incorporate several Western Digital VLSI ICs, like the WD11C00-19 SCSI protocol-support device and the WD10C20 self-adjusting data separator. Both IDCs operate under the control of an onboard 8085 μP that has 8k bytes of EPROM for program storage and 2k bytes of RAM for workspace and data buffers.

Some drive manufacturers are embedding SCSI controllers in their products. One example is the Micropolis 1370 Series. This line comprises five 5¼-in. Winchester drives with respective formatted capacities of 77M, 96.3M, 115.5M, 134.8M, and 154M bytes, using the ESDI between the drive and the embedded controller. The host interface, common to all models, is a high-performance module that conforms to the ANSI standard for the SCSI. It contains a 16k-byte dual-port FIFO buffer with full parity. The buffer eliminates the need for sector interleaving and provides a data-transfer rate of 1.5M bytes/sec to the host. The module implements all SCSI command sets for disk operation, and it can operate with the Common Command set. **EDN**

Article Interest Quotient
(Circle One)
High 503 Medium 504 Low 505

For more information . . .

For more information on the disk-controller products described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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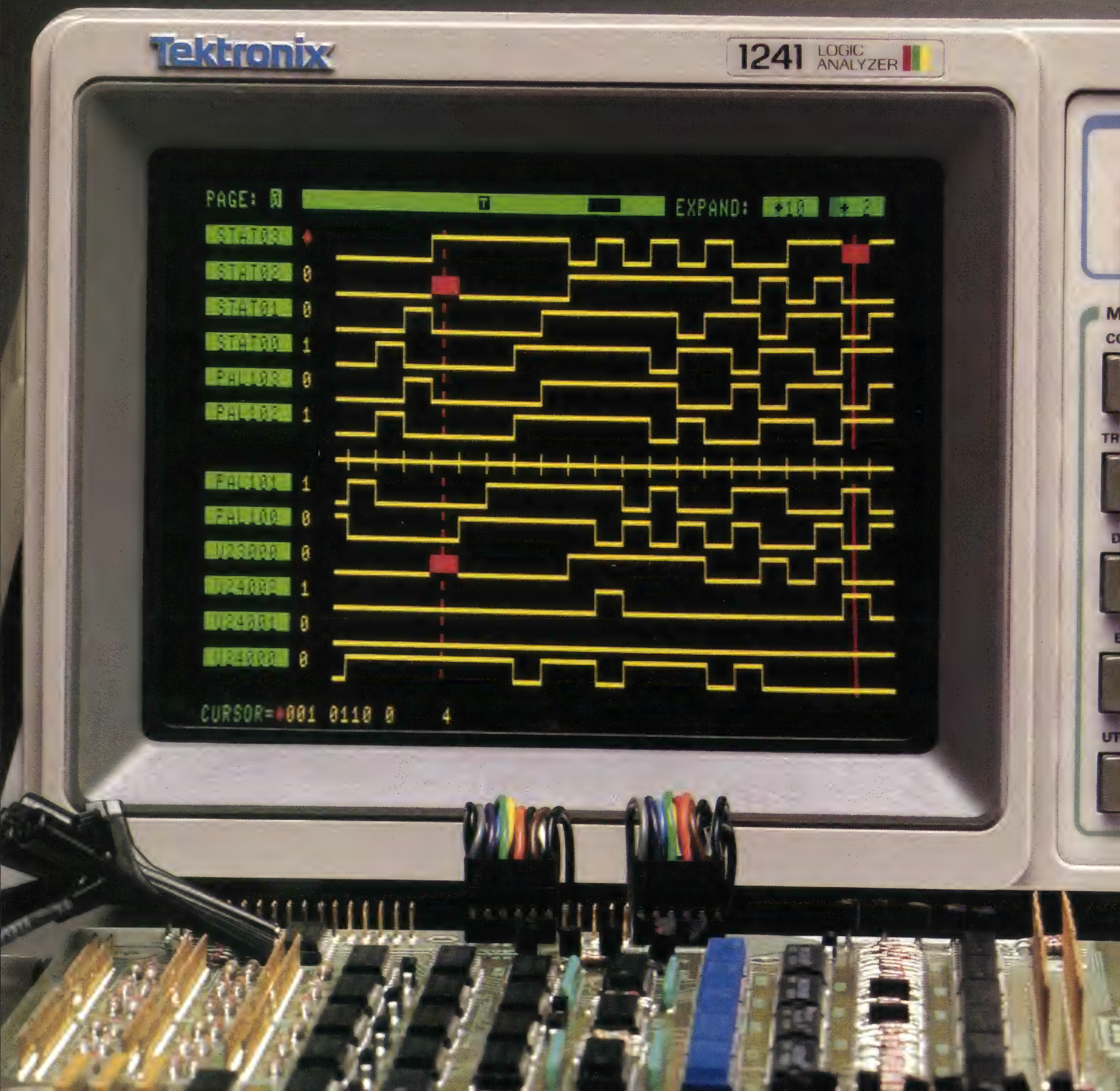

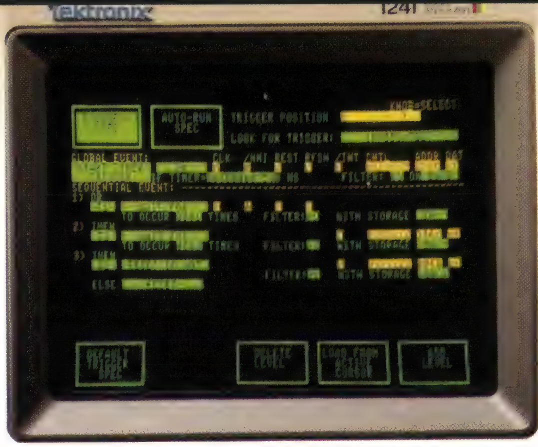

Meet the new 1241—one more reason why Tek's versatile 1200 Series offers you the best of the leading logic analyzers:

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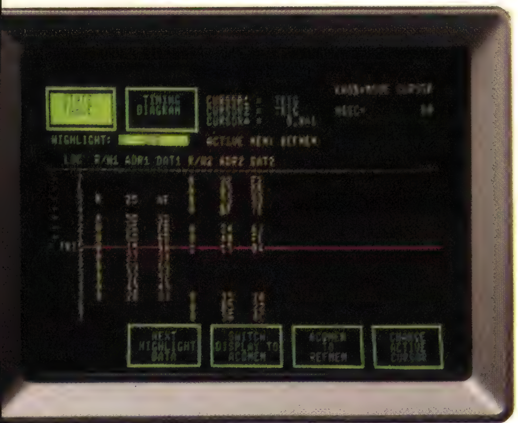

shows what your hardware and software are doing at the same time. For integrating partitioned designs, only the 1200 Series' Dual Timebase feature accurately depicts real-time interactions between independently-clocked modules. This lets you monitor relationships between two processors, or between hardware and software. Combine Dual Timebase with performance analysis on the 1241 to analyze the entire system and software performance. Monitor, for example, the range of time spent by one processor waiting for a service request response from a second processor. The 1241's histogram display and 10ns resolution make these measurements clear and precise.

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Circle No. 128 for Literature

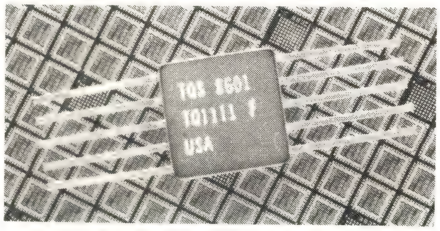
Circle No. 167 for sales application

4-bit gallium arsenide ripple-counter IC accommodates clock rates as high as 3 GHz

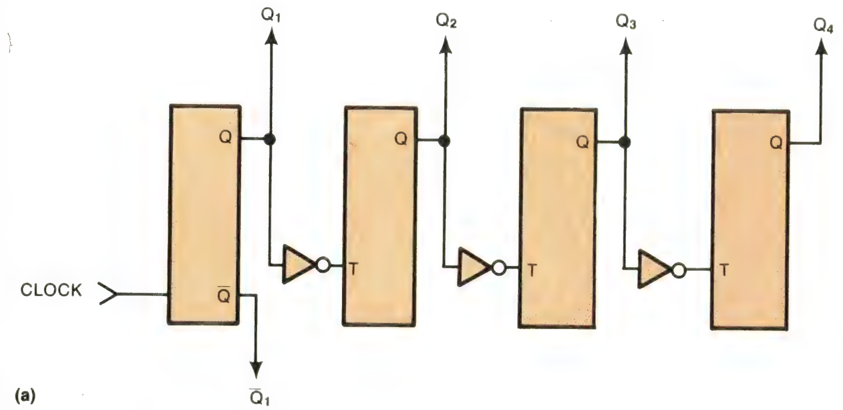
First in a planned series of GaAs MSI components, the TQ1111 family of 4-bit ripple counters (**Fig 1a**) is available in selections that accommodate 2-, 2.5-, and 3-GHz clock frequencies (Models TQ1111-20, -25, and -30, respectively). The counters, which are suitable for prescaler and high-speed counting applications, use cells from the manufacturer's standard-cell library of depletion-mode GaAs devices.

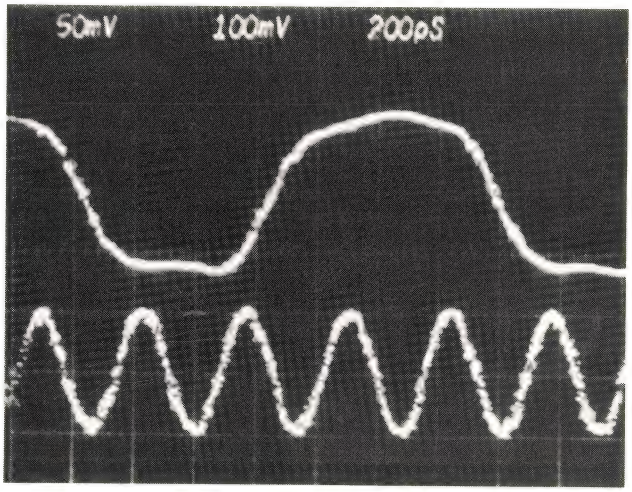
Providing full compatibility with 10K and 100K ECL circuits, the TQ1111 units spec −1 to −1.1V logic-high input levels and −1.5 to −1.6 logic-low levels. The devices operate over a wide range of power-supply voltages: Both the positive and negative supplies can vary over the absolute range of 4 to 5.2V.

Each divider stage provides an ECL-compatible output; the first divide-by-2 stage also provides a complementary output. The ac-coupled clock input requires 1V p-p min drive for the 2- and 2.5-GHz devices and 2V p-p min for the 3-GHz selection. Delay from clock edge to each output of the divide-by-2 counter is 700 psec. **Fig 1b** shows the results of a divide-by-4 operation at a 3-GHz clock frequency.



Taking advantage of the company's standard-cell library *of depletion-mode GaAs devices, the TQ1111 ripple counter has high tolerance for power-supply variations. Note the rectilinear arrays at various places on the wafer; they're test cells that the company uses to characterize and control its process.*





(b)

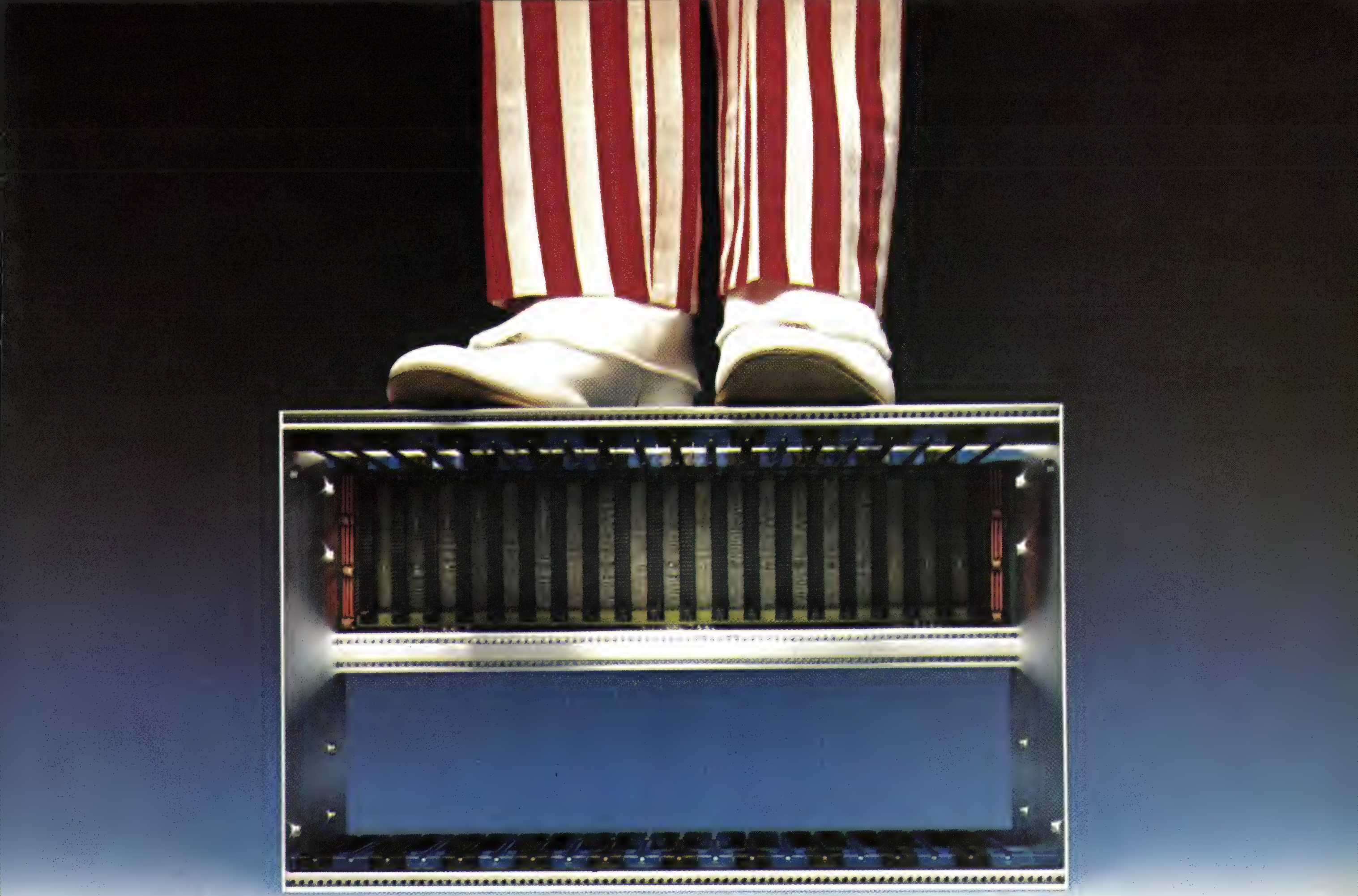
Fig 1—First in a planned family of GaAs ICs, *the TQ1111 Series 4-bit ripple counters* ***(a)*** *from Tri-Quint (a Tektronix company) operate from clock rates as high as 3 GHz. The scope photo in* ***b*** *shows the TQ1111's divide-by-4 output waveform in response to a 3-GHz clock input.*

Two other products in the manufacturer's GaAs Q-Logic IC series are slated for imminent announcement. The TQ1121 Series includes a 1.5- and 2-GHz divide-by-4/5 dual-modulus divider that's compatible with both ECL and TTL systems. Model TQ1112 is a 4-bit synchronous up/down counter that counts at 1 GHz.

Packaged in a 10-pin metal-ceramic flat pack, the TQ1111 Series operates over 0 to 85°C; devices fully specified for operation over −55 to +125°C will be available in less than a year. Prices for the 3-, 2.5-, and 2-GHz counters are $199, $119, and $89 (100), respectively. An evaluation board for the 3-GHz device costs $275.—***Bill Travis***

Tri-Quint Semiconductor Inc, Box 4935, Beaverton, OR 97075. Phone (503) 629-4227. TLX 4742021.

Circle No 745



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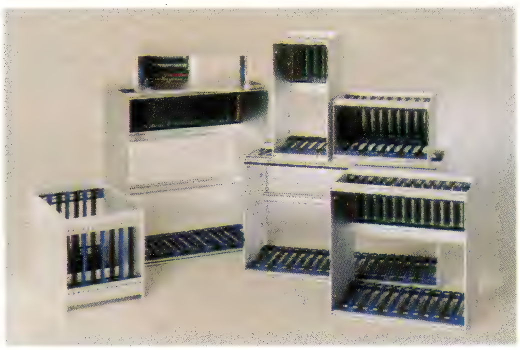

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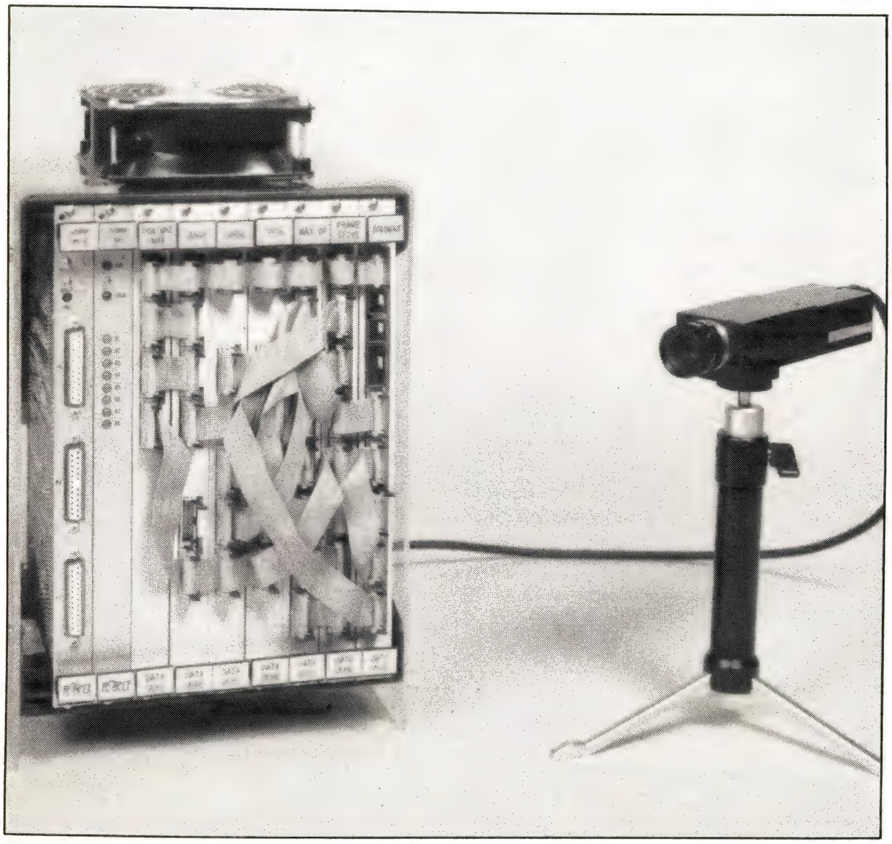
CIRCLE NO 106

VME Bus-compatible modules provide a variety of image-processing operations

Three VME Bus-compatible modules—MAX-XFS, Interpolator, and Addgen-1—acquire digitized images from a video camera and perform signal-processing tasks that transform, enhance, manipulate, and extract information from an image. The 3-module set can also directly rotate, scale, and translate an image. Because the boards communicate with CPU and memory cards in VME Bus computers, you can adapt the video-processing cards to a variety of computer systems, such as robotic manipulators, inspection systems, and process controllers.

The boards, which are the latest additions to the manufacturer's Maxvideo family of modules, perform frame-storage, interpolating, and address-generating tasks. The MAX-XFS frame-storage module stores two complete video frames in read-write memory. You can choose a MAX-XFS module that stores frames with 384×512-pixel resolution or one that stores frames with 512×512-pixel resolution. Both modules provide 8-bit storage for each pixel's video data. The modules can read each frame's data in either row or column order—in other words, they can rotate an image by 90° in real time.



***Video image-processing circuits on VME Bus cards** let a computer system capture images from a TV camera. When you combine the MAX-XFS, Addgen-1, and Interpolator cards with other video-processing cards and computer cards, the resulting system provides a variety of image-processing operations, including rotation, filtering, image enhancement, and edge highlighting.*

The Interpolator module provides an onboard subpixel interpolation algorithm that manipulates eight values with a sinc math function. By calculating new values for each pixel's video data as you zoom or scale an image in noninteger steps, the Interpolator board provides smooth transitions between adjacent pixels. To use the Interpolator board to perform first-order transformations, you must use the manufacturer's Addgen-1 address-generator module.

The MAX-XFS, Interpolator, and Addgen-1 boards communicate among themselves and other Maxvideo boards over a set of external Maxbus signal lines on the front of each card. The Max-XFS and Addgen-1 cards also connect to the VME Bus for communication with standard VME Bus-compatible computer cards. The Interpolator card uses the VME Bus only for power and ground signals. All Maxvideo cards occupy a dual-height VME Bus slot.

The manufacturer offers seven additional Maxvideo video-signal processing cards that furnish linear and nonlinear signal processors, A/D and D/A converters, and histogram and feature extractors for VME systems. In 384×512-pixel format and in single-board quantity, the MAX-XFS card sells for $3125, the Interpolator card for $3125, and the Addgen-1 card for $1200. In the 512×512-pixel format, the prices are $3750, $3750, and $1450, respectively. You must specify the pixel format when you order the cards.

—Jon Titus

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New *BergStik II* Headers with GXT can help you achieve the highest standards of reliability. Their drawn-wire pins provide smooth contact surfaces on all four sides. And the sharp corners produced by the drawn-wire process make excellent wire wrapping points providing a gas-tight connection.

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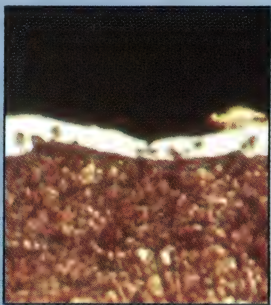
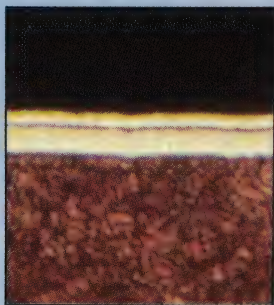


Gold plated pin surface after 25,000 cycles. Note breakdown of hard gold showing undercoat and base metal.



***BergStik II* pin surface plated with DuPont GXT.** Still smooth and unbroken after 25,000 cycles. (Cutaways of pins are microphotographs)

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The *BergStik II* Header line is versatile. Headers can be broken to any length you may desire, reducing

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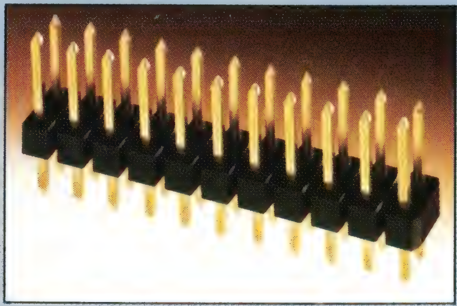

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3/31 Monday	8-9:30 AM	GRUMMAN AIRCRAFT SYSTEMS Bayles Rd., Melville, NY
3/31 Monday	10:30-12 AM	GRUMMAN AIRCRAFT SYSTEMS Stewart Ave., Bethpage, NY
3/31 Monday	1:30-3:30 PM	SPERRY CORPORATION Marcus Ave., Great neck, NY
4/1 Tuesday	8:30-12 AM	HAZELTINE CORPORATION Cuba Hill Rd., Greenlawn, NY
4/1 Tuesday	2-4 PM	EATON AIL 45 Oser Ave., Hauppauge, NY
4/2 Wednesday	9-11 AM	LORAL ELECTRONIC SYSTEMS Ridge Hill, Yonkers, NY
4/2 Wednesday	2-4 PM	IBM CORPORATION Rt. 34, Yorktown, NY
4/3 Thursday	9-11 AM	IBM CORPORATION Boardman Rd., Poughkeepsie, NY
4/3 Thursday	1-3 PM	IBM CORPORATION South Rd., Poughkeepsie, NY
4/4 Friday	8:30-11:30 AM	IBM CORPORATION Neighborhood Rd., Kingston, NY
4/4 Friday	2-4 PM	IBM CORPORATION Rt. 52, Hopewell Jctn., NY
4/7 Monday	9-10:30 AM	PERKIN-ELMER CORPORATION 100 Wooster Hts. Rd., Danbury, CT
4/7 Monday	1-1:45 PM	PERKIN-ELMER CORPORATION 50 Danbury Rd., Wilton, CT
4/7 Monday	2:30-4 PM	PERKIN-ELMER CORPORATION Main Ave., Norwalk, CT
4/8 Tuesday	8:30-10 AM	NORDEN DIVISION UAC Norden Place, Norwalk, CT
4/8 Tuesday	11-12 AM	ITT ADVANCED TECHNOLOGY CENTER 1 Research Dr., Shelton, CT
4/8 Tuesday	2-3:30 PM	GENERAL DATACOMM INDUSTRIES Straights Tpk., Middlebury, CT
4/9 Wednesday	9-11:30 AM	RAYTHEON COMPANY W. Main Rd., Portsmouth, RI
4/9 Wednesday	2-4 PM	THE FOXBORO COMPANY 28 Neponset Ave., Foxboro, MA
4/10 Thursday	9-11:30 AM	DATA GENERAL 4400 Computer Dr., Westboro, MA
4/10 Thursday	1:30-3:30 PM	DIGITAL EQUIPMENT CORPORATION 333 South St., Shrewsbury, MA
4/11 Friday	8:30-10 AM	DIGITAL EQUIPMENT CORPORATION 146 Main St., Maynard, MA
4/11 Friday	10:45-12 AM	DIGITAL EQUIPMENT CORPORATION Parker St., Maynard, MA
4/11 Friday	2-4 PM	DIGITAL EQUIPMENT CORPORATION 200 Forest St., Marlboro, MA
4/14 Monday	9-11:30 AM	SANDERS ASSOCIATES 95 Canal St., Nashau, NH
4/14 Monday	1-2:15 PM	SANDERS ASSOCIATES Rt. 3, Merrimack, NH
4/14 Monday	3-4:30 PM	SANDERS ASSOCIATES Pope Tech Pk., River Rd., Hudson, NH
4/15 Tuesday	9-10:30 AM	RAYTHEON COMPANY 350 Lowell St., Andover, MA
4/15 Tuesday	2-4 PM	AT&T TECHNOLOGIES/BELL LABS 1600 Osgood St., N. Andover, MA
4/16 Wednesday	9-11:30 AM	WANG LABORATORIES 1 Industrial Pk., Lowell, MA

DATE	TIME	SITE
4/16 Wednesday	1:30-3 PM	COMPUGRAPHIC CORPORATION 200 Ballardvale St., Wilmington, MA
4/17 Thursday	8:30-9:45 AM	COMPUTERVISION CORPORATION 14 Crosby Dr., Bedford, MA
4/17 Thursday	10:30-12 AM	HEWLETT-PACKARD CO. 175 Wyman St., Waltham, MA
4/17 Thursday	2-4 PM	PRIME COMPUTER INC. 500 Old CT Path, Framingham, MA
4/18 Friday	9-11 AM	RAYTHEON COMPANY Boston Post Rd., Sudbury, MA
4/18 Friday	12:30-2 PM	RAYTHEON COMPANY Boston Post Rd., Wayland, MA
4/18 Friday	3-4 PM	RAYTHEON COMPANY Glen St., Marlboro, MA
4/21 Monday	8:30-10:30 AM	GENERAL ELECTRIC CO. Broad St., Utica, NY
4/21 Monday	11-12 AM	GENERAL ELECTRIC CO. French Rd., Utica, NY
4/21 Monday	2-4 PM	GENERAL ELECTRIC CO. Farrell Rd., Syracuse, NY
4/22 Tuesday	9-11 AM	GENERAL ELECTRIC CO. Court St., Syracuse, NY
4/22 Tuesday	2-4:30 PM	IBM CORPORATION Glendale Dr., Endicott, NY
4/23 Wednesday	9-11:30 AM	IBM CORPORATION Bodle Hill Rd., Owego, NY
4/23 Wednesday	2-3:30 PM	NCR CORPORATION 950 Danby Rd., Ithaca, NY
4/24 Thursday	9-11 AM	XEROX CORPORATION 800 Phillips Rd., Webster, NY
4/24 Thursday	1-3 PM	XEROX CORPORATION 1350 Jefferson Rd., Henrietta, NY
4/25 Friday	9-12 AM	EASTMAN KODAK CO. 901 Elmgrove Rd., Rochester, NY
4/25 Friday	2-4 PM	HARRIS RF COMMUNICATIONS DIVISION 1680 University Ave., Rochester, NY
4/28 Monday	8:30-9:45 AM	GOULD INC., INSTRUMENTS DIVISION 3631 Perkins Ave., Cleveland, OH
4/28 Monday	10:30-12 AM	GOULD INC., OCEAN SYSTEMS DIVISION 18901 Euclid Ave., Cleveland, OH
4/28 Monday	2-3:30 PM	BAILEY CONTROLS CO. 29801 Euclid Ave., Wickliffe, OH
4/29 Tuesday	9-11 AM	ALLEN-BRADLEY CO. 747 Alpha Dr., Highland Heights, OH
4/29 Tuesday	2-4 PM	GOODYEAR AEROSPACE CORPORATION 1210 Massillon Rd., Akron, OH
4/30 Wednesday	9-10:30 AM	NCR CORPORATION 1000 Cochran Ave., Cambridge, OH
4/30 Wednesday	2-4 PM	AT&T TECHNOLOGIES NETWORK SYSTEMS 6200 E. Broad St., Columbus, OH
5/1 Thursday	8:30-10:30 AM	CINCINNATI ELECTRONICS 2630 Glendale-Milford Rd., Cincinnati, OH
5/1 Thursday	2-4 PM	AT&T TECHNOLOGIES BELL LABS 6612 E. 75th St., Indianapolis, IN
5/2 Friday	9-11:30 AM	MAGNAVOX ELECTRONIC SYSTEMS CO. 1010 Production Rd., Ft. Wayne, IN
5/2 Friday	1:30-3:30 PM	ITT AEROSPACE/OPTICAL DIVISION 3700 E. Pontiac St., Ft. Wayne, OH

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	33	45	22	0	0	7.8	7.2
Pot-Core	0	11	67	22	0	0	9.1	9.2
Laminate (power)	0	33	50	17	0	0	7.3	8.6
CONNECTORS								
Military panel	11	11	22	56	0	0	10.9	6.0
Flat/Cable	14	50	22	14	0	0	5.0	4.2
Multipin circular	7	36	22	14	14	7	10.6	7.3
PC	22	11	45	22	0	0	7.3	5.4
RF/Coaxial	0	40	30	30	0	0	8.0	7.0
Socket	23	38	31	8	0	0	4.5	3.6
Terminal blocks	17	55	11	17	0	0	4.7	3.8
Edge card	14	50	29	7	0	0	4.4	4.3
Subminiature	43	14	43	0	0	0	3.7	8.0
Rack & panel	17	0	83	0	0	0	6.7	4.2
Power	20	40	20	20	0	0	5.6	3.3
PRINTED CIRCUIT BOARDS								
Single-sided	0	67	33	0	0	0	4.0	4.1
Double-sided	0	62	38	0	0	0	4.3	5.5
Multilayer	10	30	50	10	0	0	6.2	9.5
Prototype	0	87	13	0	0	0	2.8	3.9
RESISTORS								
Carbon film	43	33	24	0	0	0	2.6	3.6
Carbon composition	30	35	35	0	0	0	3.5	4.9
Metal film	36	41	23	0	0	0	2.6	6.5
Metal oxide	33	45	11	11	0	0	3.6	4.3
Wirewound	11	44	39	6	0	0	4.9	6.3
Potentiometers	14	43	29	14	0	0	5.4	6.5
Networks	25	50	19	6	0	0	3.5	6.2
FUSES	53	35	12	0	0	0	1.6	2.1
SWITCHES								
Pushbutton	38	23	39	0	0	0	3.5	4.5
Rotary	6	47	41	6	0	0	5.2	6.6
Rocker	33	22	45	0	0	0	4.0	6.5
Thumbwheel	20	30	40	10	0	0	5.4	7.8
Snap action	38	25	25	12	0	0	4.5	5.8
Momentary	34	33	33	0	0	0	3.3	5.0
Dual in-line	29	28	29	14	0	0	5.1	5.0
WIRE AND CABLE								
Coaxial	36	57	7	0	0	0	1.7	3.8
Flat ribbon	50	43	7	0	0	0	1.4	2.4
Multiconductor	30	50	20	0	0	0	2.6	4.7
Hookup	60	35	5	0	0	0	1.1	1.8
Wire wrap	57	29	14	0	0	0	1.7	2.6
Power cords	25	58	17	0	0	0	2.5	3.6
Other	0	33	67	0	0	0	6.0	6.4
POWER SUPPLIES								
Switching	0	30	60	10	0	0	7.0	8.6
Linear	9	18	64	9	0	0	6.9	6.5
CIRCUIT BREAKERS	15	15	47	23	0	0	7.7	6.0
HEAT SINKS	29	24	47	0	0	0	4.2	4.0

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
General purpose	31	44	19	6	0	0	3.4	5.5
PC board	10	60	20	10	0	0	4.4	7.0
Dry reed	25	13	50	12	0	0	6.3	5.7
Mercury	17	17	50	16	0	0	7.0	6.5
Solid state	15	31	31	23	0	0	6.8	7.7
DISCRETE SEMICONDUCTORS								
Diode	26	35	29	10	0	0	4.6	4.6
Zener	35	21	35	9	0	0	4.6	5.7
Thyristor	36	21	29	14	0	0	5.0	6.3
Small signal transistor	38	6	44	12	0	0	5.6	6.3
FET, MOS	29	14	21	29	7	0	8.4	6.7
Power, bipolar	36	0	37	27	0	0	7.2	7.8
INTEGRATED CIRCUITS, DIGITAL								
CMOS	32	18	32	9	9	0	6.7	8.4
TTL	26	5	48	21	0	0	7.2	7.2
LS	33	11	17	39	0	0	7.8	6.8
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	33	0	56	11	0	0	6.2	7.3
OP amplifier	19	14	38	29	0	0	7.9	6.6
Voltage regulator	26	11	42	21	0	0	6.9	6.0
MEMORY CIRCUITS								
RAM 16k	45	22	22	11	0	0	4.0	4.9
RAM 64k	50	30	10	10	0	0	3.0	4.3
RAM 256k	42	33	17	8	0	0	3.3	5.3
ROM/PROM	45	22	22	11	0	0	4.0	6.9
EPROM	40	20	20	20	0	0	5.2	6.2
EEPROM	45	0	33	22	0	0	6.2	8.0
DISPLAYS								
Panel meters	9	46	27	18	0	0	6.0	5.6
Fluorescent	40	0	20	40	0	0	8.0	7.0
Incandescent	43	0	43	14	0	0	5.7	3.4
LED	29	24	35	12	0	0	5.2	4.5
Liquid crystal	12	13	37	38	0	0	9.3	6.7
MICROPROCESSOR ICs								
8-bit	34	8	50	8	0	0	5.5	7.2
16-bit	30	0	50	20	0	0	7.2	8.4
FUNCTION PACKAGES								
Amplifier	14	29	43	14	0	0	6.3	5.3
Converter, analog to digital	0	27	40	33	0	0	9.1	6.2
Converter, digital to analog	0	25	50	25	0	0	8.5	6.2
LINE FILTERS	25	25	13	37	0	0	7.5	8.0
CAPACITORS								
Ceramic	30	30	35	5	0	0	4.2	4.9
Ceramic monolithic	29	43	21	7	0	0	3.7	4.7
Ceramic disc	27	33	33	0	7	0	5.1	5.6
Film	14	43	36	7	0	0	4.9	6.3
Electrolytic	18	41	35	6	0	0	4.6	6.1
Tantalum	11	33	34	22	0	0	6.9	7.3
INDUCTORS	0	50	50	0	0	0	5.0	6.7

Source: *Purchasing* magazine's electronic business survey

"The PM 3305 digital storage scope - an engineers dream machine"

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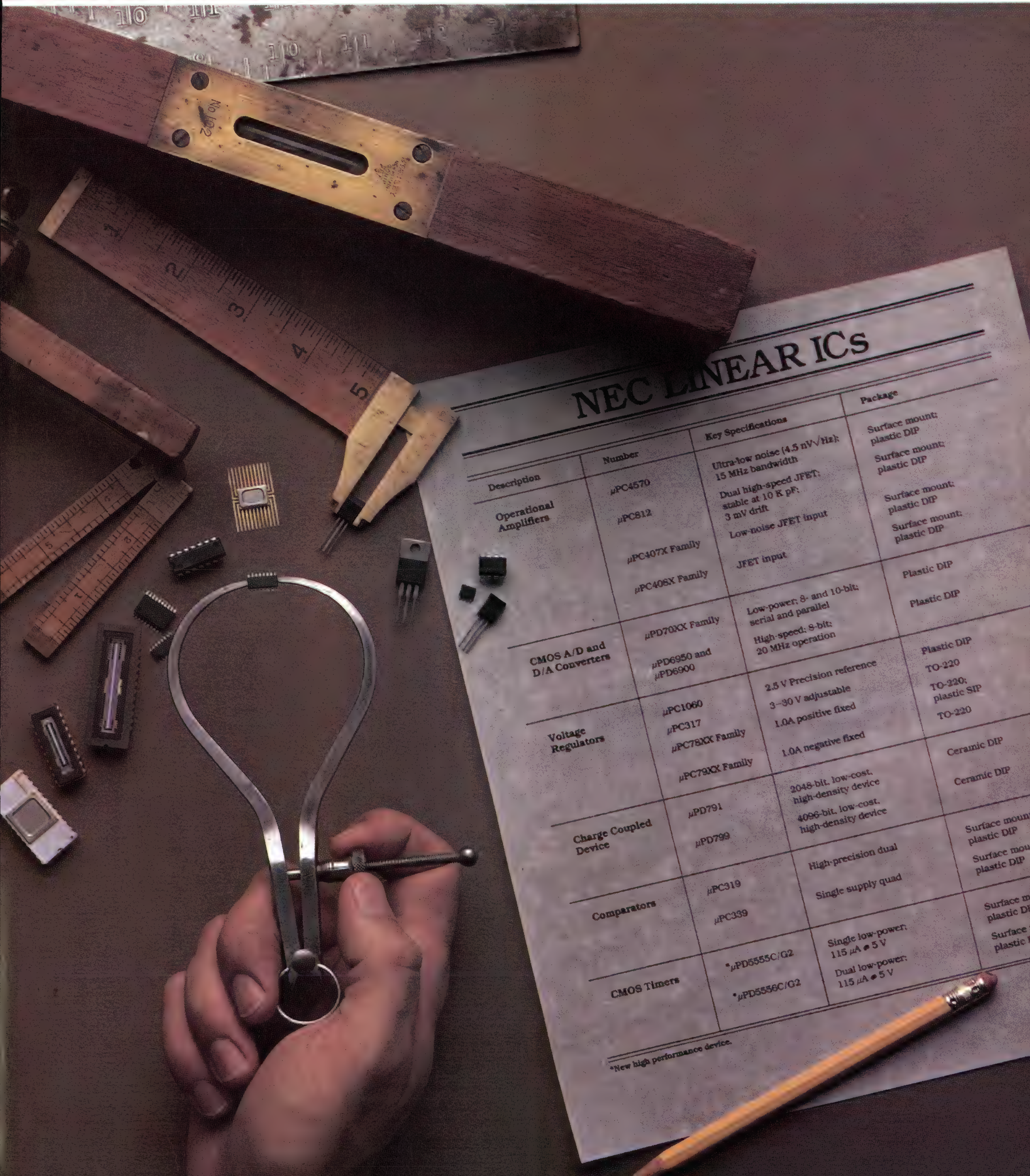

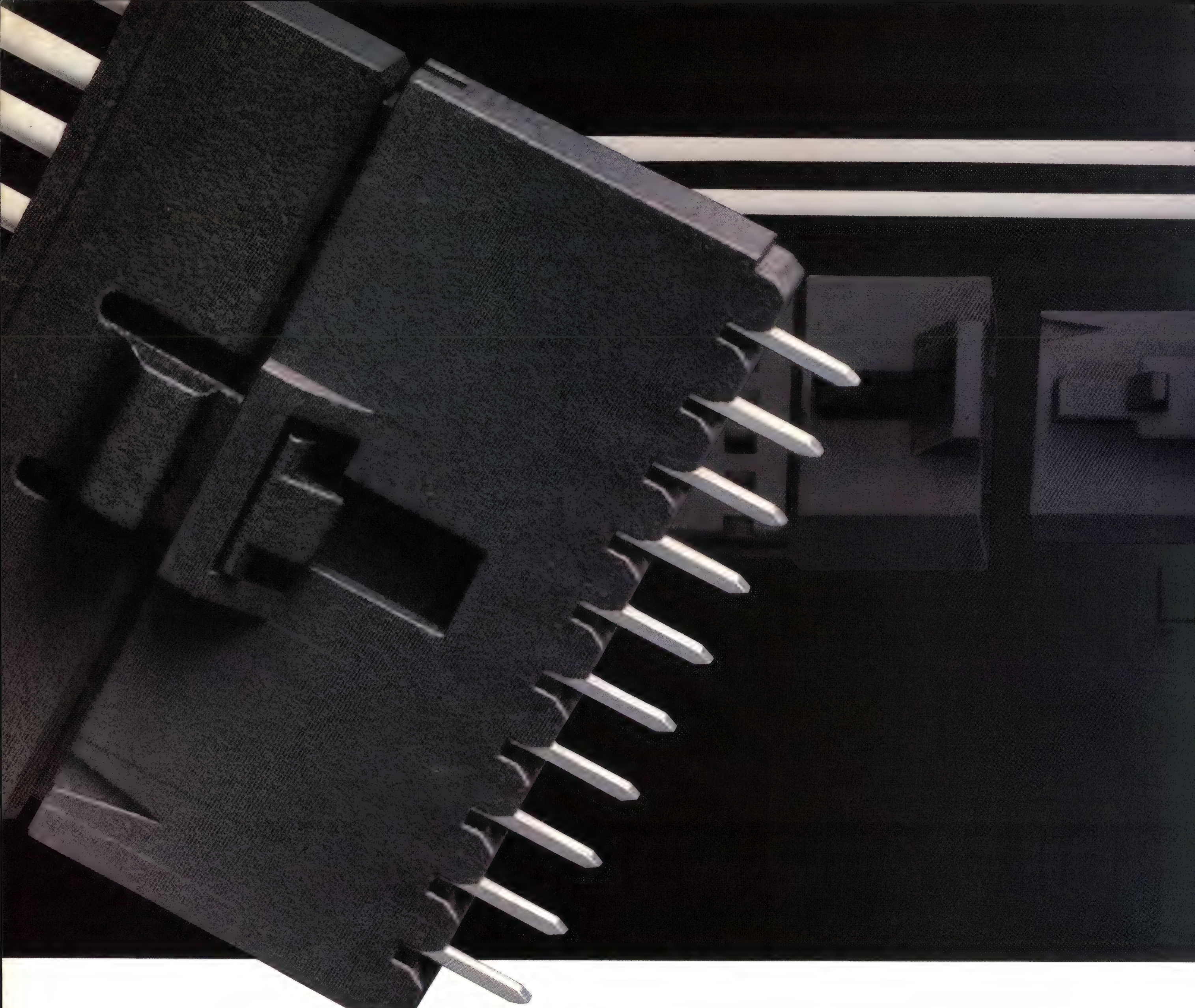

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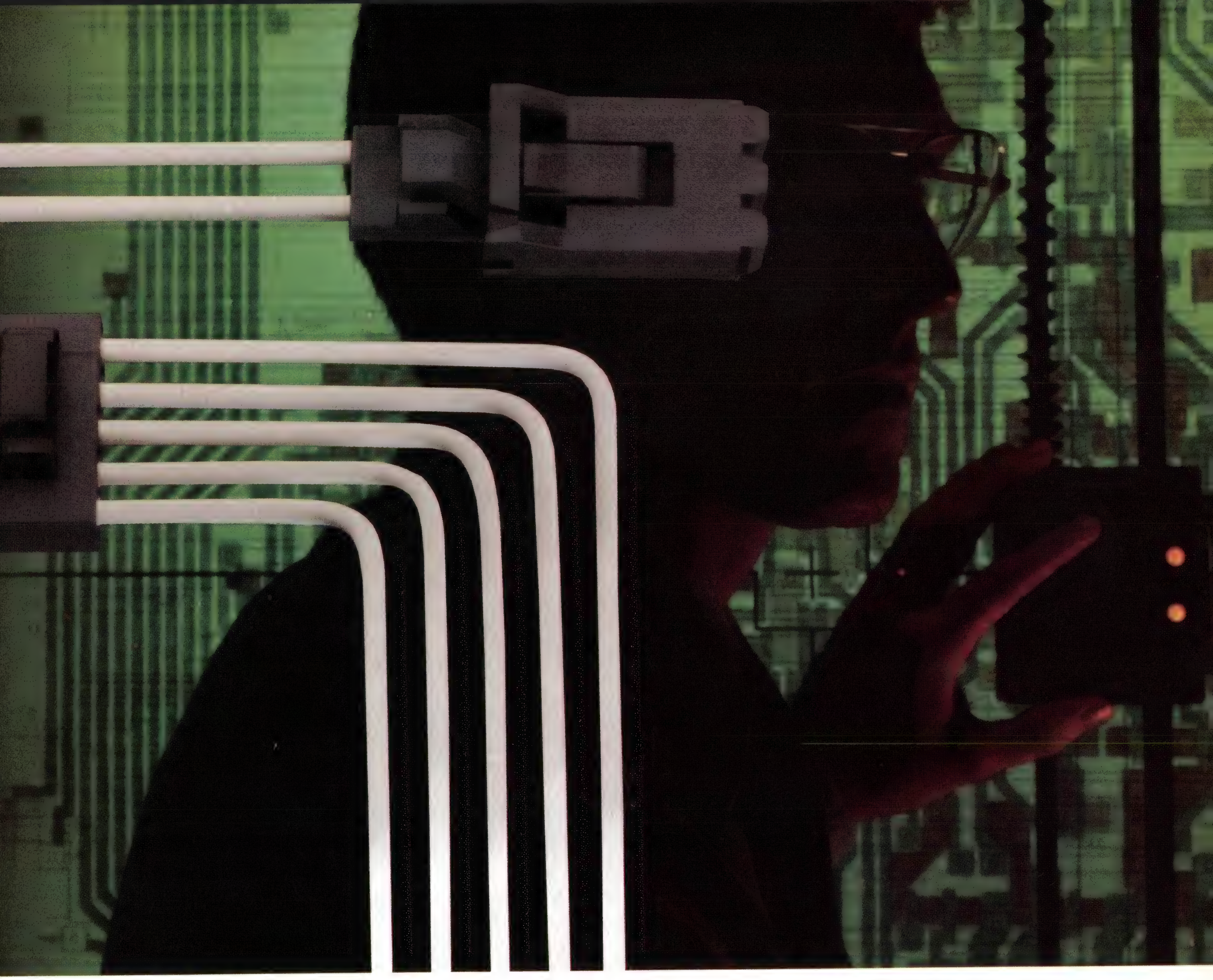
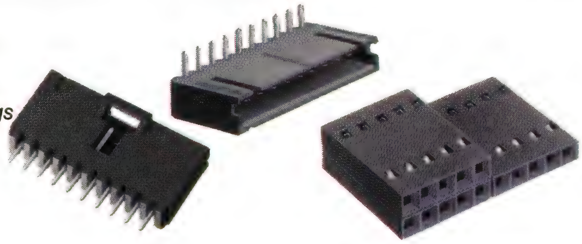
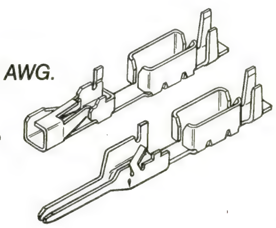




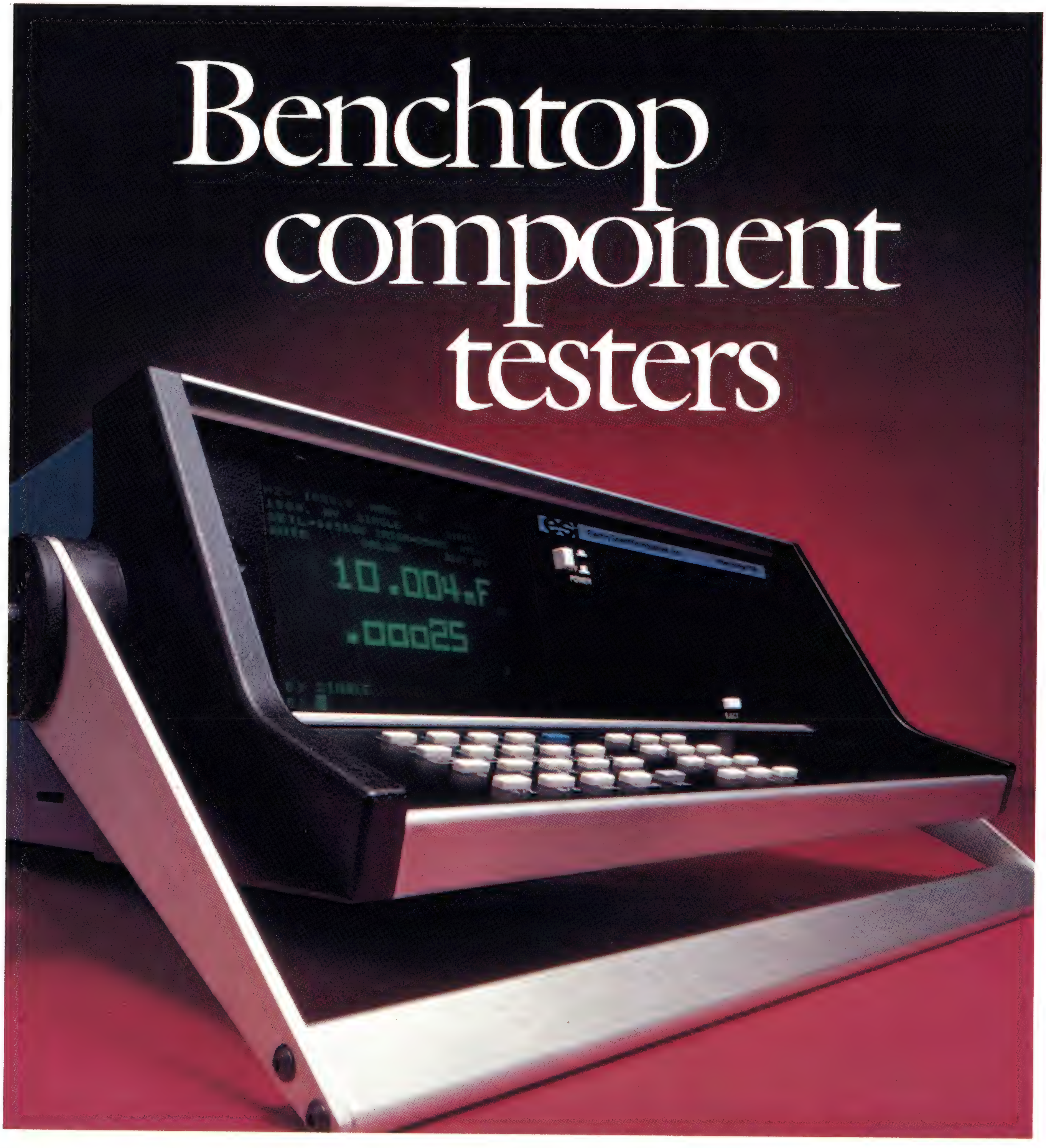
Vertical and right-angle headers, receptacles, and shrouded housings provide modular approach.



Do it all in two contact sizes—22-26 AWG and 26-30 AWG. Dual-beam contacts are overstress-protected, and feature post stops for use on long posts.

No matter how well you design a product, it will fail if your company builds it with substandard parts. Benchtop component testers are the first-line troops in the struggle for reliable, high-quality components. Relatively inexpensive and easy to use, benchtop testers mesh neatly with a new manufacturing philosophy.

Benchtop component testers



Charles H Small, *Associate Editor*

A change in testing philosophy is profoundly affecting the way electronics companies deal with their component suppliers—and that change is focusing the limelight on benchtop component testers. The new philosophy has forced these instruments to evolve from simple, go/no-go testers into units that provide a thorough battery of tests for analog and digital components.

In the past, electronics companies would try to line up as many alternate sources for components as possible. They would then test every component, on a go/no-go basis, at incoming inspection. This constant, high volume of testing mandated large, expensive testers having very high throughput. By dealing with a large number of mediocre suppliers, the companies hoped that at least one would be producing acceptable components at any given time.

Now, larger electronics companies have concluded that, to obtain better parts, they must work more closely with fewer suppliers. The larger companies therefore characterize a new component or new technology thoroughly, but only long enough to make sure that the supplier can deliver acceptable components. Then the larger companies scale back, or eliminate altogether, continual testing at incoming inspection.

Curiously, this change in philosophy by the larger companies—who, after all, have the clout to make suppliers toe the line—means that both the larger *and* the smaller companies need the updated, more flexible, smaller component testers. The larger companies need them because benchtop testers are generally easier to set up and program than larger testers. What's more, the latest testers do much more than pass parts on a go/no-go basis. As a consequence, the companies can more easily and thoroughly experiment with a new device or technology.

Smaller companies traditionally used the simple benchtop component testers for incoming inspection. These units were more affordable than the high-

***Companies are replacing simple go/no-go incoming inspection** of components with a more thorough characterization that aims to improve the quality of incoming parts. Today's benchtop component testers are evolving to meet these more thorough testing needs. (Photos courtesy Electro Scientific Industries)*

Companies used to deal with many alternate-source suppliers and hope that at least one would be producing acceptable components at any given time.

throughput testers used by large companies. The large companies' change in testing practices, however, compels the smaller companies to keep up. It's therefore fortunate that benchtop component testers have developed greater capability, because the benchtop variety is the only kind inexpensive enough to fit the smaller companies' proportionally smaller budgets.

Whether you work for a small company or a large one, you can often upgrade the quality of incoming components merely by buying a tester; you don't actually have to use it. As soon as your suppliers get wind of the fact that you've bought a tester, you might find yourself suddenly getting better components.

Despite the push for higher quality and the attendant need for testers that can evaluate components according to an engineer's specifications, most design engineers are unfamiliar with benchtop component testers and are often surprised at how capable these small units can be. For example, many benchtop component testers now have a communications port so that you can accumulate statistics on lots of parts. Tracking the failure rates of different lots of parts from different manufacturers is essential when implementing the new philosophy of working closely with suppliers.

Of the benchtop component testers covered in this article, design engineers are unlikely to use any but the semiconductor curve tracers in their day-to-day work. Most benchtop testers slave away in incoming inspection departments far from the view of design engineers. Nevertheless, design engineers might encounter those testers while consulting with the test department when first selecting the tester, or while working with a component engineer who's qualifying a new component or new technology. In these cases, the only issue of importance to the design engineer is the accuracy and thoroughness of the tester. For example, the trend toward greater accuracy at lower voltage levels puts pressure on the capabilities of analog-device testers. At the other end of the spectrum, power FETs must be tested at higher voltage levels than equivalent bipolar transistors; not all analog-device testers can impress 800V or more across a device under test.

Analog design engineers, however, need to be interested in more than the tester's performance specs. Analog designs often require the sorting and grading of analog devices according to a special, in-house specification. Therefore, analog design engineers need to be concerned with the programmability of testers as well. Many benchtop testers have their own programming languages, which are mostly enhanced versions of Basic with specialized commands for operating the tester's hardware. In addition, you can often obtain menu-driven test-generation programs that allow you to copy a device's specs directly off the spec sheet and then automatically generate a program.

Digital devices are more amenable to standardized tests and require less custom programming. Consequently, many tester makers have libraries of tests for digital devices. However, these libraries contain only tests for well-established, standard parts. The libraries lag behind the leading edge of new product introductions, and the libraries will obviously never contain custom, application-specific ICs (ASICs). You can obtain testers for ASICs, but you must program the tests yourself.

One curious omission from the libraries of standard parts is routines for testing one-time-programmable (OTP) devices before they're programmed. If an expensive OTP device like a field-programmable logic sequencer (FPLS) fails your tests after you've programmed it, the device's manufacturer could understandably be reluctant to accept the device back; your device programmer could have damaged the chip. However, you can check out some manufacturers' OTP devices before you blow the devices' fuses (some device manufacturers make the test setups available to all, some only to favored customers).

Benchtop component testers constitute an extensive variety of instruments. Some are general-purpose instruments and adapt to analog and digital devices through the use of plug-in family boards and specific device adapters. Some focus on either analog or certain types of digital devices, still others on passive devices only. Last, some testers test a single type of device, like reed relays or transformer coils, and some are so specialized that they perform only a single test on one kind of component.

In the general-purpose category, Analog Devices' LTS-2000 Series benchtop testers handle a wide range of components. The series comprises four basic mainframes that accept plug-in family boards for certain classes of components, and socket assemblies for specific devices within a family. The testers automatically calibrate themselves hourly and, with the aid of a calibration board, can exhibit 16-bit accuracy traceable to the National Bureau of Standards (NBS).

LTS-2000 Series units can test 24-pin digital ICs, linear and data-conversion ICs, and passive and discrete parts. The company also provides libraries of preprogrammed device tests on floppy disks. Further,

A family of device-specific fixtures *adapts the GenRad 1734 to testing of both analog and digital devices.*

Handling virtually all analog and digital devices, *the Analog Devices LTS 2020 boasts 16-bit accuracy.*

you can program the testers yourself in two ways: using an enhanced Basic, or responding to prompts from a menu-driven test-program generator. When testing the setup and hold times of digital ICs, the testers spec a 0.5-nsec resolution and 1.5-nsec accuracy. When testing analog devices, the testers can take measurements with 14-bit (±¼-bit) resolution.

Family modules interchange

The Deltest Model 3300 mainframe costs $37,500 and, like Analog Devices' tester, accepts a variety of family modules and device adapters. Packages of device-family modules, device adapters, and software range in cost from $3000 to $13,000. In addition to a package for digital-device families, the company has a linear-family package that tests op amps, comparators, and voltage regulators. Additional packages handle thyristors (including triacs and power diodes), diodes and transistors, and A/D and D/A converters.

Of special note is a package for such high-voltage devices as diodes, transistors, and FETs. When equipped with the package, Model 3300 can apply 1600V to the device under test (most benchtop testers presently apply no more than 600V). Also available is a general-purpose package that adapts to a variety of specialized devices: optocouplers, timers, passive hybrids, transconductance op amps, RS-232C line drivers and receivers, analog switches, transistor arrays, reed relays, and Norton amplifiers.

Eagle Test Systems' $55,000 Guardian system provides dc and parametric testing of digital, linear, and hybrid devices. The system's control computer uses the multitasking Concurrent CP/M-86 operating system and has 512k bytes of RAM. A 10M-byte Winchester disk is optional.

The Guardian's test head has a 16-bit μP and a 512k-byte memory as well. It has 32 drive/sense pins that you can expand to as many as 64. The test head's resolution for parametric measurements is 2 nsec. The company provides libraries of test programs for digital-logic chips, op amps, voltage regulators, A/D and D/A converters, and memory devices.

GenRad's 1730 Series of benchtop testers comprises a multipurpose tester and several units dedicated to digital, linear, and memory devices. The $37,000 Model 1735 tests digital and analog ICs that have as many as 24 pins. The standard system handles most SSI and MSI digital chips (including TTL, CMOS, NMOS, and ECL devices), op amps, voltage regulators, comparators, and current mirrors. Options extend the tester's coverage to A/D and D/A converters, line drivers and receivers, transistors and diodes, analog switches and multiplexers, and optocouplers.

The company includes tests for more than 400 digital devices and 800 analog devices in its library of test programs. You can upgrade a 1735 in the field to a Model 1731M networked tester for analog ICs (the M suffix indicates that the tester communicates over the company's proprietary Scan network). The 1735's test programs and device-family boards also work with the company's 1731 analog-IC tester and 1732 digital-IC tester.

GenRad's Scan network links testers over a 9600-baud, multidrop serial line to a host computer. Scan software also supports bar-code readers to aid in tracing lots of parts. The network facilitates off-line programming of the testers, access to program libraries, failure-data logging, and data analysis.

The $4995 Hy-Tronix Myriad/XK Model 440 tester is,

The trend now is to do a thorough characterization of a new component initially and then scale back, or eliminate altogether, continual testing at incoming inspection.

by far, the smallest instrument in its class. It's so small that you could consider it to be a pocket-sized tester rather than a benchtop unit. It measures 5½×3×2 in. and weighs 1 lb. Despite its small size, the Myriad/XK comes preprogrammed to test more than 25,000 standard digital devices.

Standard tests include routines for MOS logic families. The 440 can handle devices having as many as 40 pins. You can either select a code for the part under test if you know its designation, or you can have the tester identify and check out an unknown part. Optional tests cover CMOS digital parts, RAMs, and ROMs. Optional adapters allow you to test ECL parts and such analog devices as op amps and comparators.

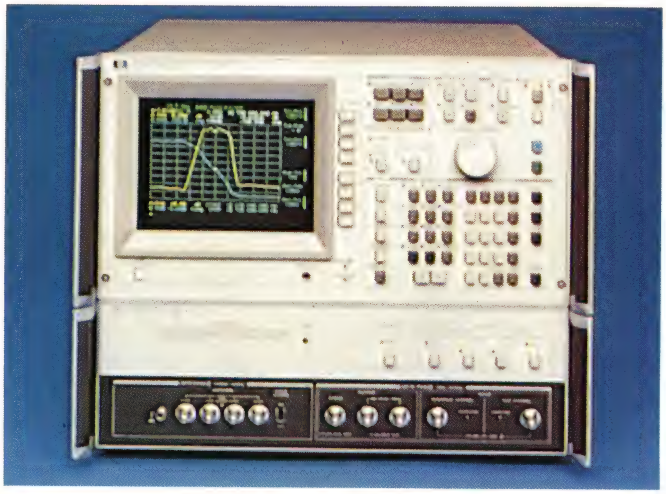
Pragmatic Test Systems' PTS-1010/15 testers differ from all other general-purpose benchtop testers in that they use an IBM PC as a control computer; all other testers discussed in this article have their own built-in μP for control. (The only difference between a PTS-1010 and a PTS-1015 is the IBM PC controller. The former uses a PC/AT, and the latter uses a PC/XT.)

The PTS-1010/15 testers spec 16-bit resolution. You can program the testers in an enhanced Basic, or you can use the company's library of test programs to test op amps, comparators, converters, and voltage regulators. The PTS-1010 costs $49,950; the PTS-1015, $42,950.

Unlike other programmable testers, which can only execute interpreted Basic test programs, the SZ-Testsysteme M3000 can execute compiled Pascal programs. The M3000 comprises a 68010-based computer and a separate test station. The computer has 1M byte of RAM and dual, 3½-in. floppy disks. In addition to enabling custom programming in Basic and Pascal, the M3000 supports menu-driven test-program generation. The instrument also accepts device adapters for passive components, relays, voltage regulators, diodes (including zener diodes), timers, optocouplers, transistors, converters, op amps and comparators, and digital components.

The Testronics Model 201A performs six basic tests on a range of discrete devices. The instrument measures leakage current, breakdown voltage, conducting voltage, gain, and gate parameters. The tester handles transistors (including FETs), SCRs, triacs, LEDs, optocouplers, diodes, and zener diodes.

You program the tester using menus, English-like commands, and function keys. The 201A uses Hewlett-Packard desktop computers for control and comes with software for collecting statistics and for operation as a



Going beyond simple RLC measurements, *the HP 4194 impedance analyzer measures the transmission characteristics of such complex passive devices as crystal resonators and filters.*

device handler. Depending on the controller selected and the physical configuration of the system, costs range from $19,985 to $40,400. Options include a 2000V/200A module for testing power devices.

After the few general-purpose testers come a welter of more narrowly targeted instruments. Digital-device testers primarily work with established SSI and MSI families. A few test microprocessors, and still others track the leading edge of technology, handling ASICs and other new device types.

EPRO has two benchtop automatic testers dedicated to digital devices. Model 140 is a general-purpose logic and memory-device tester, and Model 146 is an LSI tester that can generate test vectors at rates to 10 MHz. The 146's pattern generator can execute loops and subroutines, to make the best use of the available pattern memory. The 146 can also execute programs previously generated for Sentry testers.

You can think of the Fluke 9000 Series benchtop μP testers as in-circuit emulators that have been adapted to field service. The series comprises three models: the nonprogrammable 9005, which executes programs from ROM; the programmable 9010A; and the IEEE-488 compatible 9020A, which is designed to work with other instruments as part of an ATE system. Costs for the testers range from $2995 to $4595; for μP-specific interface pods, costs range from $995 to $2495 each.

The units in the series test μPs indirectly. You replace the μP in your system under test with a Series 9000's test probe—just like hooking up an in-circuit emulator to a prototype. The instrument then runs a

With a built-in tape drive for loading programs, *the Electro Scientific Industries Model 2160 Video Bridge displays readings and setups on its CRT.*

In addition to low-level analog *and digital devices, the Deltest 3300 tests high-voltage devices.*

series of tests to exercise the system that the µP was controlling. The tester checks the µP's bus, RAM, ROM, and I/O. You can also program the tester to conduct custom test sequences.

GenRad's $48,500 1732 digital-IC tester comes equipped to test 24-pin devices. You can expand it with additional drive/sense pins to handle 40- or 48-pin devices. Each of the tester's pins has an associated 4k×4-bit memory for storing test vectors. The unit can therefore test complex digital parts like µPs, as well as SSI and MSI parts. Because the instrument's precision measuring unit can connect to any pin, you can do parametric tests in addition to functional tests. The 1732 has IEEE-488 and RS-232C interfaces, and it can communicate over the company's proprietary Scan network.

At $995, Micro Sciences' voltmeter-sized ICT-101 is the lowest-cost 24-pin-IC tester. The instrument measures 5×12½×11½ in. and weighs 8 lbs. The basic unit handles a range of common NMOS and CMOS logic devices. Options include test heads for RAM and ROM tests as well as expansions of the tester's device library.

The Logue-McDonald $12,000 Model 323i is a functional tester for digital ICs. It works with an IBM PC for programming and gathering statistics. The unit furnishes 32 drive/sense pins and specs a 200-psec resolution. It can also program EEPROMs.

Like the company's multipurpose testers, Pragmatic Designs' PTS-1000/05 digital testers use an IBM PC as a control computer (again, the only difference is the respective use of the PC/XT and the PC/AT). The PTS-1000/05 units test 24-pin digital devices. Each instrument includes a 12-bit measuring unit for doing parametric as well as functional tests. Options include an ECL adapter, a CMOS stress-test adapter, and a ganged input-leakage adapter.

The Siemens-Allis Model 725 digital-IC tester comes configured with one device-test head; you can upgrade it in the field to handle two test heads and two device handlers at once. The 725 handles 24-pin devices. The company offers an extensive library of preprogrammed tests for most common SSI and MSI devices. Prices for the 725 range from $30,000 to $50,000.

The tester has a learn mode that enables it to check customized parts like ROMs. It will print out a summary of failures by pin and by device upon command, and it can grade components into 12 categories or "bins." When equipped with its terminal option, the 725 also serves as a host computer for program development.

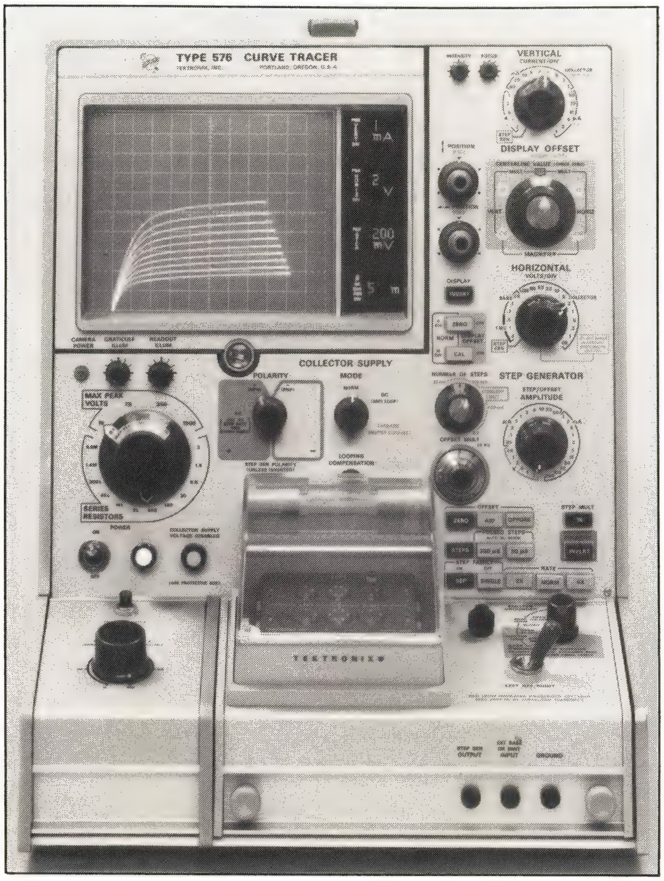
Most currently available digital testers play it safe by handling only well-established, mature chips. Others dare to venture beyond the familiar. Functional testers in Integrated Measurement Systems' Logic Master Series handle the very newest, fast, high-pin-count, custom and semicustom ICs. The testers can have a combination of as many as 192 sense or drive pins (you can link two testers for a total of 384 pins), and they deliver test vectors to the device under test at 20M vectors/sec with 1-nsec resolution (a speed of 40M vectors/sec is optional).

Each drive pin can have as much as 16k bits of

associated pattern storage. You can operate a Logic Master tester as a stand-alone unit, or you can link it with common CAE workstations. A 64-channel tester having 32 pattern-generation and 32 data-acquisition pins costs $29,500. Naturally, because the tester is designed for custom parts, the company offers no library of device programs.

Also taking aim at complex, high-speed custom chips are HiLevel Technology and Step Engineering. Both companies have been supplying development tools for bit-slice systems for many years. In order to meet the needs of bit-slice designers, HiLevel and Step have developed stimulus/response testers that feature short cycle times and large pin counts. In addition, the companies offer logic analyzers that work in parallel with the stimulus/response systems. Both companies plan to bring their bit-slice-instrumentation experience to bear on ASICs.

HiLevel's DTS3700 stimulus/response tester provides as many as 256 bidirectional or as many as 512 unidirectional stimulus pins, in addition to 256 logic-analysis channels and 256 real-time comparison channels. You can add or subtract pins in modular groups of 16. The instrument can accommodate 50-MHz cycle rates, and it offers 1-nsec resolution. System prices start at $30,000.



Probably the only type of benchtop component tester *that a design engineer routinely encounters, a curve tracer like the Tektronix 576 develops a family of response curves for semiconductors.*

Step's stimulus/response tester offers 64 to 512 pins and cycles at speeds to 50 MHz. A basic 64-pin module with mainframe costs $25,000. Each pin has an associated 2k-bit pattern memory that you can expand to 64k bits. Channel-to-channel skew is less than 0.1 nsec.

Though memory testers are a species of digital tester, they merit separate consideration; the nature of memory devices shifts the emphasis to different tester features. Memories from different vendors are basically alike, and users tend to acquire a relatively high volume of a few memory devices, compared with a much smaller number of other types of digital devices. As a consequence, throughput is more important than flexibility in memory testers.

EPRO offers three memory testers. Model 210 tests as many as 10 nonvolatile memory devices in parallel. Each of the tester's 10 sockets is independent; test programs proceed independently for each of the 10 devices, and one device's failure doesn't affect any of the remaining devices.

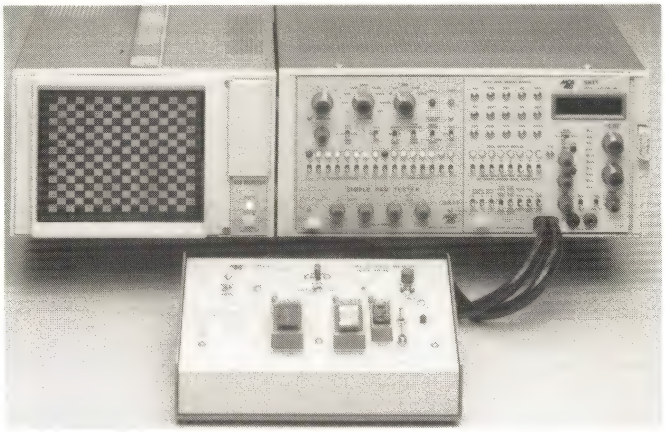
Model 302 can test two nonvolatile memory devices in parallel. The tester can execute redundancy repair algorithms, and it provides dc, parametric, programmability, and functional tests. The company also offers a version of its Model 140 LSI tester that comes equipped to test only nonvolatile memory devices.

Nonvolatile devices

Along with its many other benchtop component testers, GenRad makes the $62,500 1734 memory tester. The instrument has an 8-MHz algorithmic pattern generator. Its data path is eight bits wide, and its timing generator can produce 26 independently programmable edges with 2-nsec accuracy. You can program cycle times from 125 nsec to 5.245 μsec with 4-nsec resolution. All output pins feature programmable dynamic loading.

The $10,000 price tag on Logical Devices' Dynatest dynamic-RAM tester demonstrates the reason why some makers of the far more expensive general-purpose device testers do not compete in the RAM-tester market. The Dynatest checks RAMs' control signals—RAS, CAS, read, and write—and also checks access

Benchtop component testers can evaluate devices according to a design engineer's specs.



Most memory-device testers are automated instruments, *but the Mosaid SRT1 is a completely manual, interactive instrument suitable for engineering evaluation and failure analysis.*

timing, refresh cycles, and page-mode bit-cell patterns. It generates test vectors at rates to 100 MHz with 10-nsec resolution. The tester collects statistics and stores them on its built-in floppy disk. The tester has 12-bit RAS and CAS counters to ensure that it will be able to handle future, higher-capacity memory devices.

Even more specialized is the Mosaid SRT-1. Rather than feature extensive programmability, the SRT-1 boasts extensive manual control of the signals applied to the device under test. The tester is therefore better suited to the interactive investigation of memory-device properties by an engineer rather than the go/no-go testing needs of incoming inspection.

The instrument comprises a Tektronix TM500 mainframe and the modules that plug into it. Modules and test heads are available for both bit-wide and byte-wide memory devices. The tester displays a bit map of the device under test on a CRT. The SRT-1 can handle dynamic and static RAMs with organizations as large as 256k×1 and 64k×8 bits. It tests at speeds to 3 MHz. Depending on the configuration of the tester, prices range from $22,710 to $37,210.

The company also makes the computer-controlled MS2200 memory tester. It costs $48,000 and is able to test byte-wide memory devices with organizations as large as 4M×8 bits, and at rates to 10 MHz. The MS2200 also provides a real-time bit map. An optional measurement unit provides dc parametric testing with resolutions of 100 pA and 0.5 mV.

The Teradyne MX-19 is the only benchtop memory tester that can test two byte-wide RAMs, ROMs, EPROMs, or EEPROMs in parallel. The tester can address chips having a 1M-word×16-bit address space. You program the tester with Pascal-like test and memory-pattern languages.

Because of the wider variety of tasks analog devices must perform, analog-device testers tend to be very specialized. Few analog testers handle a very broad range of device types, although one product—GenRad's 1731 analog tester—is not so narrowly focused as other members of its category. The $35,000 1731 handles many analog and analog/digital devices with the aid of an array of adapter boards. Devices tested include op amps, current mirrors, A/D and D/A converters, comparators, regulators, line drivers and receivers, analog switches, transistors, diodes, and optocouplers. The tester can measure dc, ac, and pulsed parameters.

The remaining analog testers discussed here aim for smaller targets. For example, as the company's name suggests, FET/Test specializes in discrete analog devices. The company's $60,000 Model 9400 measures pulsed, dc, and ac (at 1 kHz) parameters of FETs. In addition, the 9400 handles discrete bipolar transistors, thyristors, and diodes. The tester provides forcing currents ranging from picoamperes to 120A and forcing voltages as high as 1.2 kV. The tester requires a $17,000 control computer for operation and programming. You program tests by selecting from a menu the parameters to be measured.

Integrated Technology's ITC 5500 measures the reverse-breakdown specifications of Schottky diodes in accordance with MIL-STD-750. The tester employs an inductive element to apply pulses of known energy to the diode under test. Because of the high energy levels involved, the instrument's test head incorporates a clear plastic shield to protect the operator from exploding devices.

For active devices, the simplest benchtop testers are curve tracers. Rather that pull out pinpointed parameters, curve tracers give you a family of response curves. Curve tracers can display a device's breakdown voltage, leakage current, gain, saturation voltage, and both forward and reverse current and voltage. Furthermore, for linear ICs, a curve tracer lets you determine offset voltage, input current, gain, CMRR, and PSRR.

Tektronix makes two curve tracers: the 576 and the 577. The 577 is lighter than the 576 and lacks the 576's storage CRT and ability to take low-current measurements. Both tracers accept a range of plug-in boards that adapt the instruments to standard devices or high-power devices.

All the analog-device testers described thus far work with active components. In contrast, LCR meters

Design engineers are unlikely to use any benchtop tester, except the semiconductor curve tracers, in their day-to-day work.

measure parameters like inductance, capcitance, resistance, and dissipation and quality factors under different combinations of applied-signal frequency, dc bias, and amplitude. The major application of LCR meters is testing passive components during incoming inspection.

Impedance analyzers are related to LCR meters. In addition to impedance measurements, impedance analyzers also take transmission measurements like gain, phase, and group delay. Impedance analyzers suit more complex passive components, like crystal oscillators, ceramic resonators, and filters.

The test frequency that an LCR meter can apply to a device under test is important, because you might want to evaluate power devices at 120 Hz (60 Hz full-wave rectified) and other devices near their working frequencies. (Be aware that high-frequency performance adds to an LCR meter's cost.)

The $2095 Boonton Model 5110 applies test signals at 100 Hz, 120 Hz, and 1 kHz. It measures capacitance from 0.1 pF to 19.99 mF, inductance from 0.1 μH to 1.999 kH, and resistance from 0.001Ω to 19.99 MΩ. It measures dissipation factor (D) from 0.001 to 1.999 and quality factor (Q) from 0.5 to 199.9. Test levels for applied voltage is 1V; a 50-mV source is available.

Electro Scientific Industries' impedance meters range from the $995 Model 252 to the $6195 Model 2160. Model 252 is a voltmeter-sized instrument that specs 0.25% accuracy. Other, more expensive models in the 252 line offer autoranging and a 120-Hz stimulus instead of a 1000-Hz stimulus.

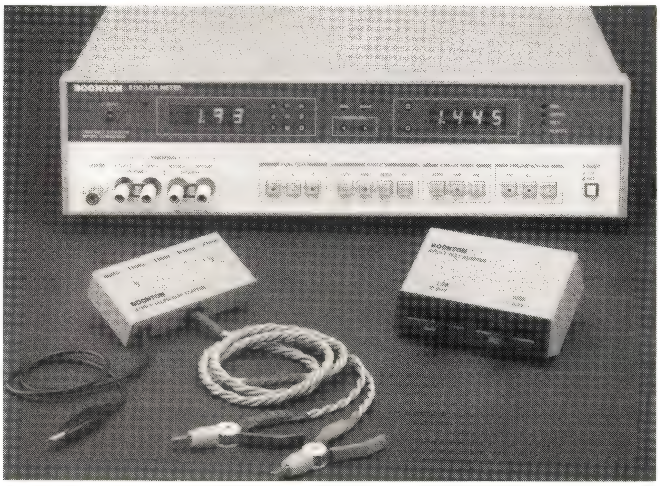
The company's Model 2150 and Model 2160 Video Bridges were the first impedance-measuring instruments to have a CRT for displaying readings and test setups. Model 2160 incorporates a tape drive for loading programs for stand-alone operation. The instruments can stimulate the device under test with more than 300 frequencies, ranging from 20 Hz to 150 kHz. Their basic accuracy is ±0.02%.

GenRad's 1600 line of LCR meters ranges in price from $1995 to $5400. Models 1657 and 1658 supply test frequencies of 120 Hz and 1 kHz. The $3400 1658 has an IEEE-488 option. The $5400 Model 1687-B supplies test frequencies to 1 MHz, and the $5200 Model 1689 is fully programmable and furnishes test frequencies to 100 kHz.

Hewlett-Packard offers six LCR meters. The line comprises the HP 4261A, HP 4262A, HP 4276A, HP 4277A, HP 4274A, and HP 4275A. In addition, the company has four impedance analyzers—the HP 4191A, HP 4192A, HP 4193A, and the HP 4194A.

The LCR meters vary in price from $2420 to $8700. The instruments' basic accuracy is 0.1%. Their stimulus-frequency ranges span, for the least-expensive 4276A, 100 Hz to 20 kHz, and for the top-of-the-line 4275A, 10 kHz to 10 MHz. The impedance analyzers vary in price from $11,600 to $19,800. Test frequencies range from 10 Hz to 1 GHz, depending on the model.

In addition to LCR and impedance meters, HP offers three instruments that prove useful for characterizing components. The $7950 HP 4140B combines a picoammeter with a precision dc source. This instrument takes charge/voltage measurements of semiconductors and leakage measurements of high-resistance materials. The $19,300 HP 4145A semiconductor-parameter ana-



Providing low-cost evaluation of passive components, *the Boonton 5110 LCR meter accepts 4-terminal Kelvin clips.*

Able to operate two test heads at a time, *the Teradyne MX-19B memory-device tester supports program development as well.*

Manufacturers of benchtop component testers

For more information on benchtop component testers, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

Acoustic Emission Technology Corp
1824J Tribute Rd
Sacramento, CA 95815
(916) 927-3861
Circle No 681

Analog Devices
Two Technology Way
Norwood, MA 02062
(616) 329-4700
Circle No 682

Boonton Electronics Corp
791 Route 10
Randolph, NJ 07869
(201) 584-1077
Circle No 683

B&W Engineering Corp
3303 Harbor Blvd, Suite E-7
Costa Mesa, CA 92626
(714) 540-9975
Circle No 684

Deltest Systems Ltd
Box 24, Pottery Rd
Poole, Dorset BH14 8RQ, UK
(0202) 745314
TLX 417264
Circle No 685

Deltest (USA)
AB Northstar Dev Inc
8800 Highway Seven, Suite 315
Minneapolis, MN 55426
(612) 933-0297
Circle No 686

Eagle Test Systems Inc
1353 Armour Blvd
Mundelein, IL 60060
(312) 367-8282
Circle No 687

Electro Scientific Industries Inc
13900 NW Science Park Dr
Portland, OR 97229
(503) 641-4141
Circle No 688

EPRO Corp
2342 Harris Way
San Jose, CA 95131
(408) 262-3912
Circle No 689

FET/Test Inc
160 Albright Way, Suite E
Los Gatos, CA 95030
(408) 374-3613
Circle No 690

John Fluke Mfg Co Inc
Box C 9090
Everett, WA 98206
(206) 347-6100
Circle No 691

GenRad Inc
300 Baker Ave
Concord, MA 01742
(617) 369-4400
Circle No 692

Hasco Components Reedtest
247-40 Jericho Tpk
Bellrose, NY 11001
(516) 328-9292
Circle No 693

Hewlett-Packard Co
1820 Embarcadero Rd
Palo Alto, CA 94303
Phone local office
Circle No 694

HiLevel Technology Inc
18902 Bardeen
Irvine, CA 92715
(714) 752-5215
Circle No 695

Hy-Tronix Instruments Inc
Box 827
Newton, KS 67114
(316) 283-5730
Circle No 696

Integrated Measurement Systems Inc
9525 SW Gemini Dr
Beaverton, OR 97005
(503) 626-7117
Circle No 697

Integrated Technology Co
1228 N Stadem Dr
Tempe, AZ 85281
(602) 968-3459
Circle No 698

Leader Instruments Corp
380 Oser Ave
Hauppauge, NY 11788
(516) 231-6900
Circle No 699

Logical Devices Inc
1321 NW 65th Pl
Fort Lauderdale, FL 33309
(305) 974-0975
Circle No 700

Logue-McDonald Automation Inc
E 10807 Montgomery, Suite 9
Spokane, WA 99206
(509) 928-5717
Circle No 701

Markenrich Corp
14946-A Shoemaker Ave
Santa Fe Springs, CA 90670
(213) 921-0250
Circle No 702

Micro Sciences Inc
3807 Cavalier Rd
Garland, TX 75042
(214) 487-6808
Circle No 703

Mosaid Inc
3375 Scott Blvd, Suite 130
Santa Clara, CA 95051
(408) 727-7199
Circle No 704

Optimized Devices Inc
220 Marble Ave
Pleasantville, NY 10570
(914) 769-6100
Circle No 705

Philips Test & Measuring Instruments Inc
85 McKee Dr
Mahwah, NJ 07430
(201) 529-3800
Circle No 706

Pragmatic Test Systems Inc
1405 S Milpitas Blvd
Milpitas, CA 95035
(408) 943-1920
Circle No 707

Siemens-Allis Inc
Box 5477
Cherry Hill, NJ 08034
(609) 424-9210
Circle No 708

Sienko Consultants Inc
Box 76
Sandy Hook, CT 06482
(203) 426-3200
Circle No 709

Step Engineering Inc
661 E Arques Ave
Sunnyvale, CA 94086
(408) 733-7827
Circle No 710

SZ-Testsysteme GmbH
Postweg 5
8201 Amerang, West Germany
(08075) 1031
TLX 17807580
Circle No 711

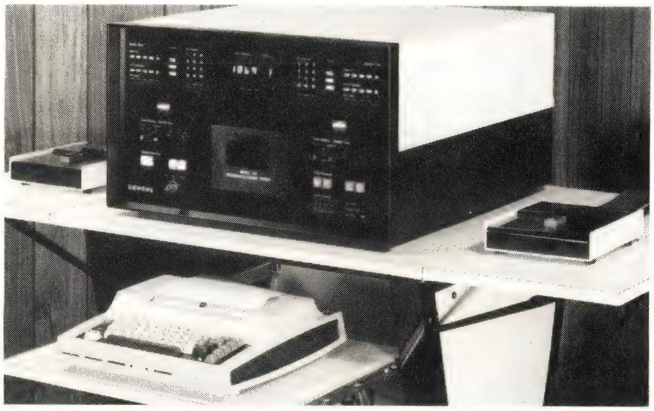
Tektronix Inc
Box 500
Beaverton, OR 97005
Phone local office
Circle No 712

Teradyne Inc
154 Middlesex Turnpike
Burlington, MA 01803
(617) 273-1850
Circle No 713

Testronics Inc
1810 N Glenville Dr
Richardson, TX 75081
(214) 238-8378
Circle No 714

Wayne Kerr Inc
600 West Cummings Park
Woburn, MA 01801
(617) 938-8390
Circle No 715

Design engineers encounter benchtop component testers either when first selecting the tester, or when working with a component engineer during component qualification.



Able to test two SSI or MSI devices simultaneously, *the Siemens-Allis Model 725 comes with device-program libraries.*

lyzer functions as both a manual curve tracer and as an automated semiconductor analyzer. The $4600 HP 4342A Q meter measures inductors' quality factors from 5 to 1000.

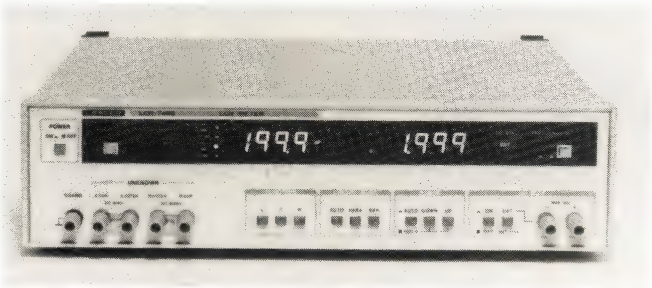
Leader Instruments' $1395 Model LCR-745G programmable LCR meter has 1% basic accuracy and applies two test frequencies: 120 Hz and 1 kHz. IEEE-488 and BCD interfaces are options.

Philips's $1195 Model PM 6303 is an autoranging LCR meter that can identify an unknown component. The instrument produces an equivalent circuit diagram appropriate to each measurement mode. It can generate, for example, the symbol for an inductor with a Q factor of less than 500, which is an inductor in series with a resistor.

Like ESI and HP, Wayne Kerr offers a line of component analyzers that ranges from a basic LCR meter to an automated impedance analyzer. The $895 Model 4220 eschews even a comparator and provides basic LCR measurements. The $12,000 top-of-the-line Model 3245 sports an amber CRT that displays readings, setups, and an equivalent circuit for the device under test.

Although solid-state devices have replaced electromechanical components in many applications, electromechanical devices are still in use. Furthermore, the relatively high failure rate of these components mandates testing, and instruments for that task are available. Optimized Devices $29,000 Model MT 301C is a general-purpose tester of electromechanical relays (including reed relays). It can handle normal, hybrid, or latching relays having ac or dc coils, and it can test as many as 20 form-A, -B, or -C contacts in a single relay. You can cycle the relay under test at rates from 10 to 3000 Hz. Like the MT 301C, the Markenrich RT250

Testing μPs indirectly *by substituting for the μP and exercising the system that the μP was controlling, the Fluke 9000 Series also supports guided-probe diagnostics.*



Because it provides an IEEE-488 interface, *Leader Instruments' LCR-745G LCR meter suits semiautomatic operation.*

handles electromechanical and reed relays.

Hasco Components Reedtest's Model 301 handles only glass-enclosed reed relays. The tester measures pickup and dropout ampere-turns as well as contact resistance. The tester also indicates if a relay fails to pick up or drop out at all.

Sienko Consultants offers the $1500 Model 2600 membrane-switch tester. The tester accommodates membrane-switch panels having as many as 26 connections. You can set the allowable contact resistance from 1 to 999Ω. The tester also detects short circuits.

Two companies make benchtop mechanical-shock generators for particle-impact noise-detection tests (PIND). Acoustic Emission Technology's PIND-2000 and B&W Engineering's BW-LPD-B2000 sell for $10,000 to $15,000, depending on options. The principle behind PIND testing is very simple: The tester shakes the device under test to see if anything loose inside rattles. PIND testing can detect very small foreign objects and loose bond wires inside a semiconductor's package. **EDN**

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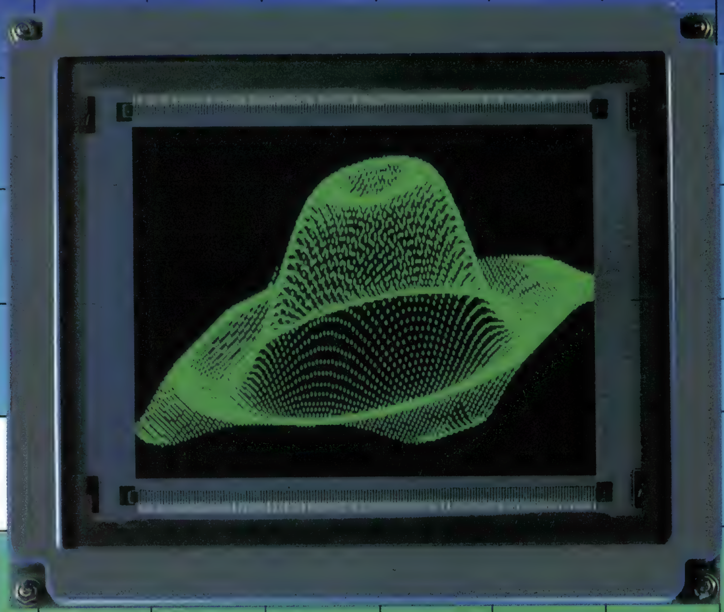
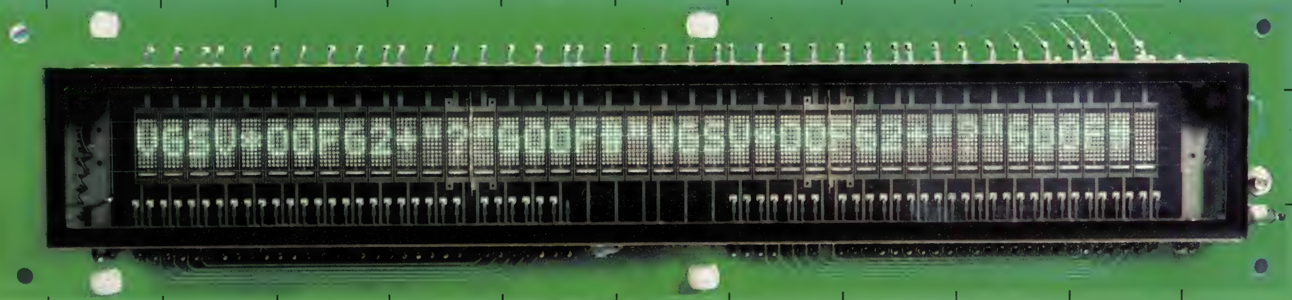
Article Interest Quotient (Circle One)
High 470 Medium 471 Low 472

Clear and Bright
Vacuum Fluorescent Technology



Graphic Module



Dot Module

FEATURES

1. High resolution and high brightness provides excellent appearance and quality.
2. Light weight and thin package permits compact design.
3. TTL compatibility provides easy interface and self-test and brightness control are standard features.

Graphic Module Series List

Type code	Number of Pixels row × column	Pixel Pitch mm	Effective Display Area mm	System	Alphabetic Display digit × col
GP1005	128 × 64	0,65	83 × 41,4	VFD	20 × 6
GP1006	256 × 64	0,65	166 × 41,4	VFD	40 × 6
GP1009	240 × 64	0,45	107,9 × 28,7	VFD	40 × 6
GP1001	320 × 120	0,375	120 × 45	FLVFD	52 × 12
GP1002	320 × 240	0,375	120 × 90	FLVFD	52 × 24

Inquire for single color Graphic Module

Dot Module Series List

Type code	Characters × Line	Dot Construction	Character Size	Nos. of displaying characters
M20SD01CA	20 × 1	5 × 7 dot	3.5 × 5.0	222
M20SD42CA	20 × 1	5 × 12 dot w/cursor	3.5 × 8.75	222
M40SD02CA	40 × 1	5 × 7 dot w/cursor	3.5 × 5.0	222
M40SD42CA	40 × 1	5 × 12 dot w/cursor	3.5 × 8.75	222
M202SD03CA	20 × 2	5 × 7 dot w/cursor	3.5 × 5.0	222
M402SD04CA	40 × 2	5 × 7 dot w/cursor	3.5 × 5.0	222

Inquire for single color Dot Module

CIRCLE NO 112

FUTABA (Europe) GmbH

CIRCLE NO 196

Am Seestern 24 · D-4000 Düsseldorf 11 · Tel. 0211/59 10 14/15 · Telex 8 585 550 fute d · Facsimile: 0211/59 31 33

TABLE 1—MANUFACTURERS ACCORDING TO DEVICE TYPE

BENCHTOP COMPONENT TESTERS

- **GENERAL PURPOSE**
  - ANALOG DEVICES
  - DELTEST
  - EAGLE
  - GENRAD
  - HY-TRONIX
  - PRAGMATIC
  - SZ-TESTSYSTEME
- **SPECIAL PURPOSE**
  - **DIGITAL**
    - **SSI/MSI**
      - EPRO
      - GENRAD
      - LOGUE-McDONALD
      - MICRO SCIENCES
      - PRAGMATIC
      - SIEMENS-ALLIS
    - **VLSI/CUSTOM**
      - HILEVEL
      - IMS
      - STEP
    - **MEMORY**
      - DELTEST
      - EAGLE
      - EPRO
      - GENRAD
      - HY-TRONIX
      - LOGUE-McDONALD
      - MICRO SCIENCES
      - MOSAID
      - PRAGMATIC
      - SZ-TESTSYSTEME
      - TERADYNE
  - **ANALOG**
    - **ACTIVE**
      - ANALOG DEVICES
      - DELTEST
      - EAGLE
      - HEWLETT-PACKARD
      - FET/TEST
      - GENRAD
      - HY-TRONIX
      - INTEGRATED TECHNOLOGY
      - PRAGMATIC
      - SZ-TESTSYSTEME
      - TEKTRONIX
      - TESTRONICS
    - **PASSIVE**
      - ANALOG DEVICES
      - BOONTON
      - DELTEST
      - ESI
      - GENRAD
      - HEWLETT-PACKARD
      - LEADER
      - PHILIPS
      - SZ-TESTSYSTEME
      - WAYNE KERR
  - **OTHER**
    - ACOUSTIC
    - B&W ENGINEERING
    - HEWLETT-PACKARD
    - HASCO
    - MARKENRICH
    - OPTIMIZED DEVICES
    - SIENKO

TABLE 2—BENCHTOP COMPONENT TESTERS

COMPANY	MODEL	ANALOG	DIGITAL	MEMORY	PASSIVE	PRICE	COMMENTS
ACOUSTIC EMISSION TECHNOLOGY	PIND-2000					\$10,000 TO \$15,000	PIND TESTER (PARTICLE-IMPACT NOISE DETECTION)
ANALOG DEVICES	LTS-2000 SERIES	•	•		•	\$31,000	DEVICE-FAMILY ADAPTERS REQUIRED, \$3000 TO \$15,000
BOONTON ELECTRONICS	5110				•	\$2095	LCR METER
B&W ENGINEERING	BW-LPD-B2000					\$10,000 TO \$15,000	PIND TESTER
DELTEST SYSTEMS	3300	•	•	•	•	\$37,500	DEVICE-FAMILY ADAPTERS REQUIRED, \$3000 TO \$13,000
EAGLE TEST SYSTEMS	GUARDIAN	•	•	•		\$55,000	
ELECTRO SCIENTIFIC INDUSTRIES	252/3/4				•	\$995 TO \$1295	LCR METERS
	2150/60				•	\$5295/ \$6195	LCR METERS WITH CRT READOUTS
EPRO	140/6		•	•		\$40,000 TO \$70,000	
	210			•		\$50,000 TO \$60,000	TESTS 10 DEVICES IN PARALLEL
	302			•		\$30,000 TO \$40,000	TESTS TWO DEVICES IN PARALLEL
FET/TEST	9400	•				\$60,000	FET TESTER
JOHN FLUKE MFG CO	9000 SERIES		•			\$2995 TO \$4595	μP TESTER
GENRAD	1731	•				\$35,000	
	1731M	•				\$36,000	
	1732M		•			\$48,500	
	1734M			•		\$62,500	
	1735	•	•	•		\$37,000	
	1657				•	\$1995	LCR METERS
	1658				•	\$3400	
	1687-B				•	\$5400	
	1689				•	\$5200	

Continued on pg 108

Superior performance now runs in the family.

Introducing the 8842A digital multimeter.

Choices. Choices.

Should you choose the powerful Fluke 8840A? Or the new, advanced 8842A?

Depending on the level of performance you need, consider this:

Enhanced capabilities for new applications.

The new 8842A is so technologically superior, it can outperform DMMs costing twice as much. Its capabilities include 0.003% 1-year basic accuracy and 100 nV resolution for dc voltage measurements. And it incorporates exclusive new thin film resistors* for a two-year calibration cycle.

The widely-accepted 8840A on the other hand, offers value unmatched by any other DMM in its class. Like the 8842A, it's simple to operate. It gives you long-term reliability. And it delivers high productivity with a low overall cost of ownership.

Choose either model for under $1,000.

The 8840A starts at $760, the 8842A at $995. With inexpensive IEEE-488 and true RMS AC options available for both models.

Which one is right for you? The choice may not be easy.

But at least now, it's a family decision.

Call toll-free 1-800-44-FLUKE (1-800-443-5853) Ask for extension 123.

Talk to our sales engineers about the 8840A and the new 8842A. Take advantage of our **no-risk 15-day trial period.**

FROM THE WORLD LEADER IN DIGITAL MULTIMETERS.

FLUKE 8840A		**FLUKE 8842A**	
0.005% basic dc accuracy (1 Yr.)		0.003% basic dc accuracy (1 Yr.)	
0.16% basic ac accuracy (1 Yr.)		0.08% basic ac accuracy (1 Yr.)	
0.013% basic ohms accuracy (1 Yr.)		0.008% basic ohms accuracy (1 Yr.)	
Resolution to 1μV dc, 10μA dc, 1mΩ		Resolution to 100nV dc, 1μA dc, 100μΩ	
One-year specifications and warranty		Two-year specifications and warranty	
8840A	$760	8842A	$995
8840A-05 IEEE-488 Interface	$150	8842A-05 IEEE-488 Interface	$150
8840A-09 TRMS AC option	$185	8842A-09 TRMS AC option	$250

FLUKE®

* Patent pending

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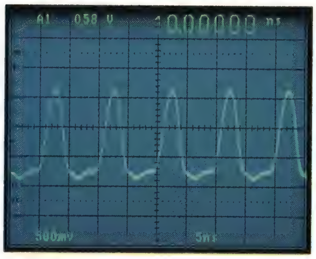
 Ad No. 2801-8842

CIRCLE NO 113

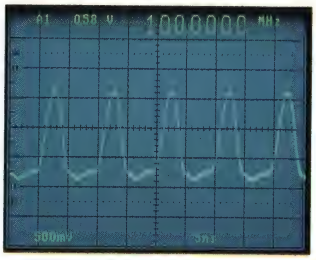
TABLE 2—BENCHTOP COMPONENT TESTERS *(Continued)*

COMPANY	MODEL	ANALOG	DIGITAL	MEMORY	PASSIVE	PRICE	COMMENTS
HASCO COMPONENTS REEDTEST	301				•	—	REED-RELAY TESTER
HEWLETT-PACKARD	4261A				•	$2420	120 Hz, 1 kHz — LCR METERS
	4262A				•	$3240	120 Hz, 10 kHz
	4274A				•	$8200	100 Hz TO 100 kHz
	4275A				•	$8700	10 kHz TO 10 MHz
	4276A				•	$3850	100 Hz TO 20 kHz
	4277A				•	$5500	10 kHz TO 1 MHz
	4191A				•	$14,320	1 TO 1000 MHz — IMPEDANCE ANALYZERS
	4192A				•	$11,590	5 Hz TO 13 MHz
	4193A				•	$7380	400 kHz TO 110 MHz
	4194A				•	$19,800	100 Hz TO 40 MHz
	4140B	•				$7950	PICOAMMETER/CURRENT SOURCE
	4145A	•				$19,300	AUTOMATIC CURVE TRACER
	4342A				•	$4600	Q METER
HILEVEL TECHNOLOGY	DTS3700		•			FROM $30,000	VLSI VERIFICATION
HY-TRONIX	MYRIAD/XK 140	•	•	•		$4995	
INTEGRATED MEASUREMENT SYSTEMS	LOGIC MASTER		•			FROM $29,000	VLSI VERIFICATION
INTEGRATED TECHNOLOGY	FTC 5500	•				—	SCHOTTKY REVERSE-BREAKDOWN TESTER
LEADER INSTRUMENTS	LCR-745G				•	$1395	120-Hz, 1-kHz LCR METER
LOGICAL DEVICES	DYNATEST			•		$10,000	RAM TESTER
LOGUE-McDONALD AUTOMATION	323i		•	•		$12,000	PROGRAMS EPROMs
MARKENRICH	RT250				•	$24,000	RELAY TESTER
MICRO SCIENCES	ICT-101		•	•		$995	
MOSAID	SRT-1			•		$22,710 TO $37,210	MANUALLY OPERATED, INTERACTIVE INSTRUMENT
	MS2200			•		$48,000	
OPTIMIZED DEVICES	MT 301C				•	$29,000	RELAY TESTER
PHILLIPS TEST & MEASURING INSTRUMENTS	PM 6303				•	$1195	LCR METER
PRAGMATIC TEST SYSTEMS	PTS-1000/05		•			—	IBM PC-BASED
	PTS-1010/15	•	•	•		$49,950/$42,950	
SIEMENS-ALLIS	725		•			$30,000 TO $50,000	
SIENKO CONSULTANTS	2600				•	$1500	MEMBRANE-SWITCH TESTER
STEP ENGINEERING	STIMULUS/RESPONSE		•			$25,000	VLSI VERIFICATION
SZ-TESTSYSTEME	M3000	•	•	•	•	—	
TEKTRONIX	576	•				—	CURVE TRACERS
	577	•				—	
TERADYNE	MX-19			•		—	
TESTRONICS	201A	•				$19,985 TO $40,400	DISCRETE-DEVICE TESTER
WAYNE KERR	4220				•	$895	LCR METERS
	4225				•	$1500	
	4210				•	$2200	
	905				•	$3495	
	6425				•	$4995	
	3245				•	$12,000	

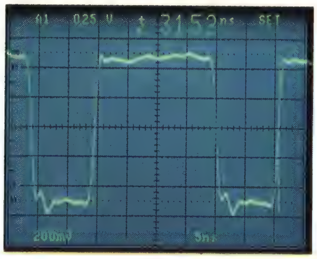
SIXTEEN TOUGH ASSIGNMENTS.



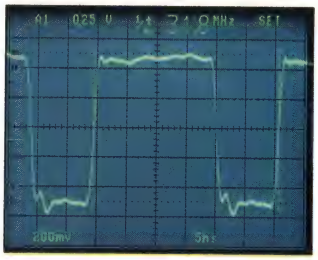
A period measurement is made on a 100 MHz clock using the extended accuracy and resolution of the Counter/Timer/Trigger in the 2465 DVS.



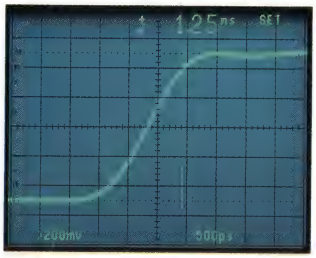
A frequency measurement is made with the same high precision. Simply press two buttons, and the period measurement on the left is converted to frequency.

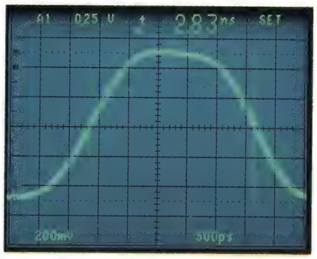


Short time intervals can be measured most accurately with the easy-to-use time cursors. They also make quick work of longer intervals, with 1% accuracy.

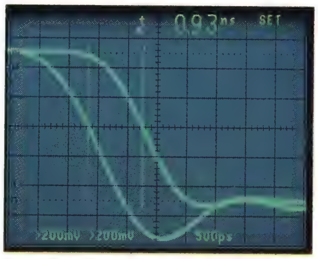


Calculated frequency takes only seconds. The time cursor measurement on the left can be converted to frequency with push-button ease and 1% accuracy.

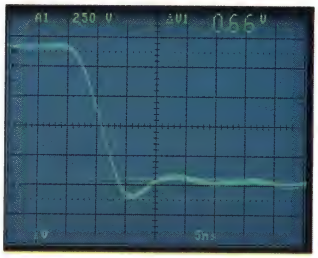




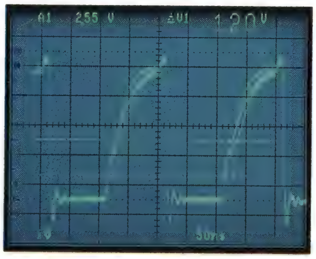
This fast-pulse rise time is nearly that of the scope. The 2465 achieves maximum bandwidth with minimum waveform aberrations. This level of pulse response ensures that **pulse width** and amplitude measurements on fast waveforms (above) truly reflect conditions in a circuit under test.



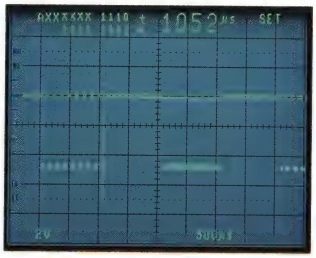
Propagation delay measurement accuracy is assured by built-in propagation delay matching. Delay between Channels 1 and 2 can be corrected to the probe tip.



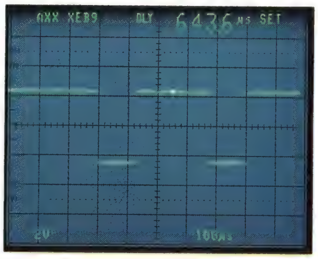
Overshoot and ringing measurement accuracy requires flat response in a probe/oscilloscope system. Tek probes and scopes are designed to work together.



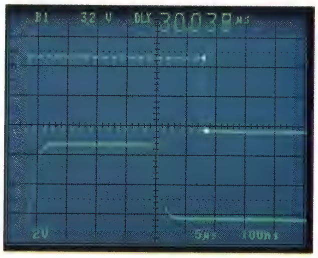
Logic-level violations can be spotted quickly on a TTL waveform (above) with measurement cursors set to define logic-level boundaries.



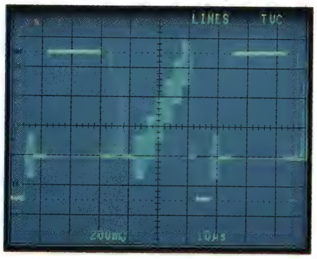
The Word Recognizer (with a binary word) is used to pick out a pulse train in a data stream. The time cursors measure pulse train duration.



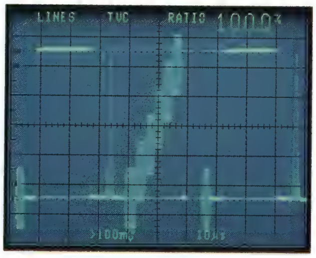
Identify a word position. The Word Recognizer (in HEX) is intensifying a word position and measuring delay relative to a waveform on another line.



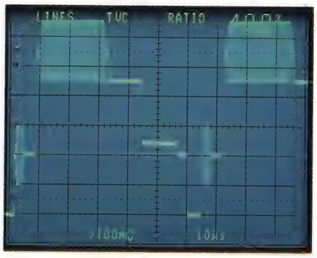
Delayed sweep is used to expand the last pulse in a pulse train. The intensified zone identifies the expanded pulse position.



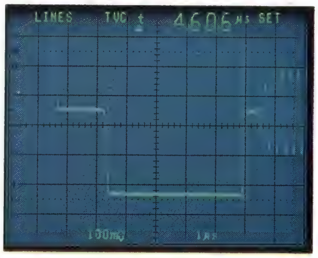
TV line trigger in the 2465 DVS displays a full-field composite test signal. The built-in TV clamp circuit removes hum and tilt on the ac-coupled video.



Calibrate cursors in IRE units with variable attenuation. Blanking level to reference white level is defined as 100 IRE units in NTSC video.

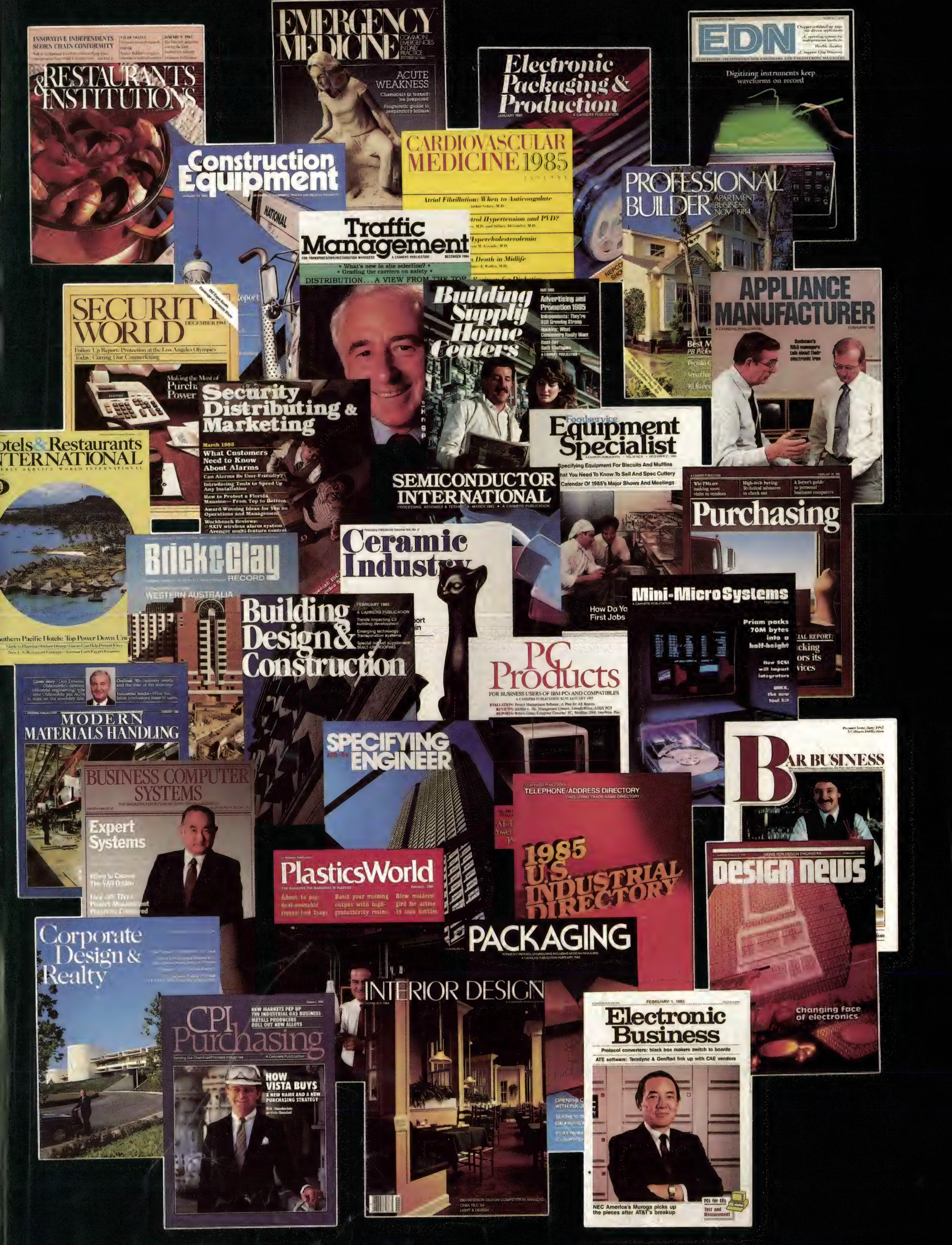


Burst amplitude should be 40 IRE units in NTSC video. The cursors quickly measure other waveform amplitudes. Field triggering checks any line.



Sync width and blanking are common, easy-to-make timing measurements. Accurate time measurements can be made anywhere in a video system.

 PMA-628



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Digitizing instruments keep waveforms on record
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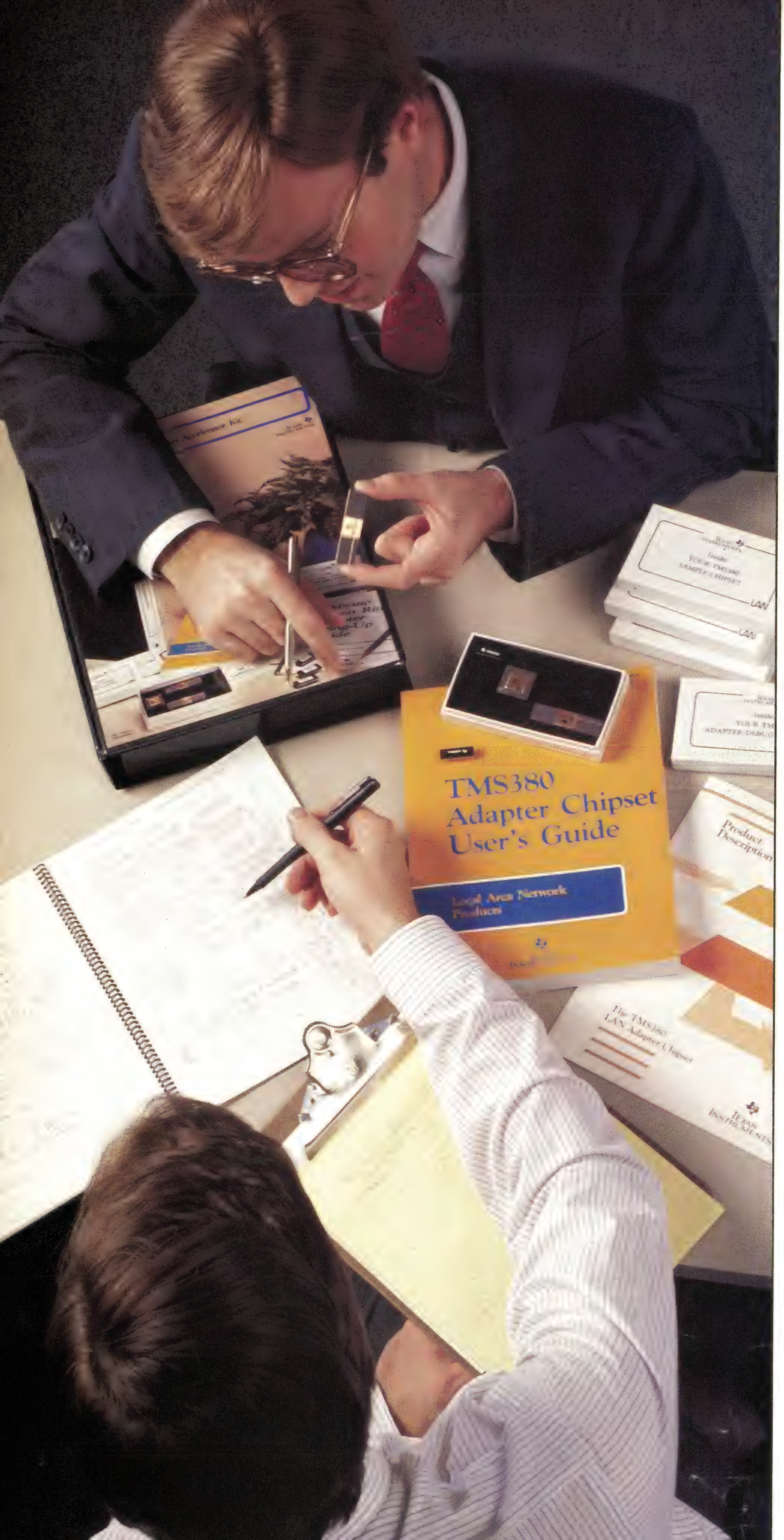


Design in TI's new

The new IBM® Token-Ring Network promises to become the industry standard. And if you are wondering about the best and quickest way to tie your product into this new 4-Mb/sec LAN, here's your solution: **The TMS380 chip set from Texas Instruments.**

TI's TMS380 is the *only* commercial chip set tested — and system-verified — by IBM. It's *the* silicon standard for this new high-speed office-system LAN.

And for a sure, fast entry into this exciting new market, you can begin with TI's TMS380 *Design-in Accelerator Kit.*

Q. What kinds of products can communicate through the new LAN?

A. With the TMS380 chip set, almost any.

TI's new TMS380 chip set was developed jointly with IBM. Its general-purpose system interface allows many kinds of equipment from various manufacturers to communicate through the IBM Token-Ring Network. And since this is an open network, any product in which you use the TMS380 can communicate with any other, when common languages are used.

Q. Is expensive cabling required?

A. No.

Your customers have the option of using telephone twisted pair or shielded twisted pair. And the point-to-point topology of the token ring makes it ideal for fiber optics, since the taps that are necessary with bus topologies are not required.

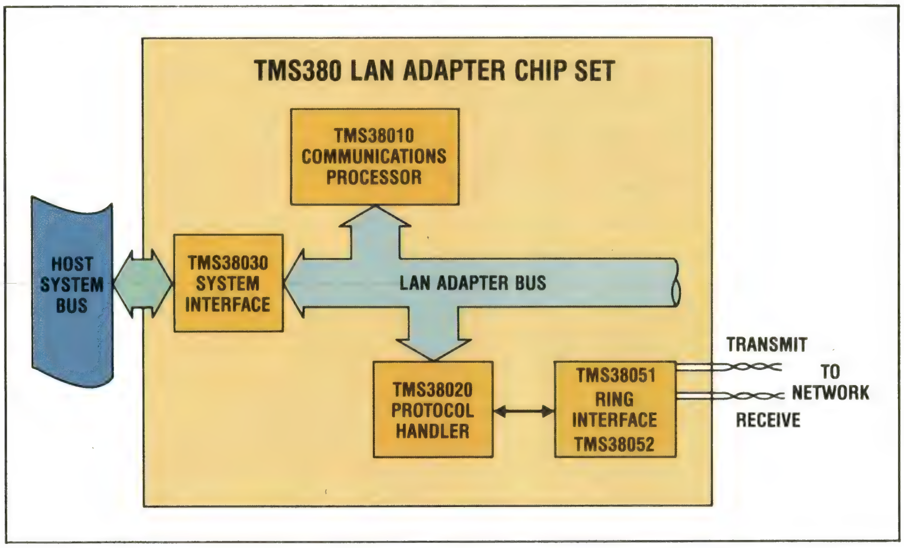
Q. Where does TI's TMS380 chip set fit in?

A. It's the heart of your LAN adapter card or subsystem.

The TMS380 chip set is a complete solution for the physical interface and media-access control. Its integrated LAN-adapter architecture provides for efficient, transparent handling of the IEEE 802.5 protocols. TI's TMS380 in your product will give your customers freedom to choose the cabling system that best suits their needs. And the flexibility to interface with any of the popular logical-link-control and higher-layer protocols.

◀ **Everything you need** to begin designing your own IBM Token-Ring Network LAN adapter is included in your TI *Design-in Accelerator Kit:* Three TMS380 chip sets, comprehensive literature, and debug software.

IBM compatibility with token-ring-LAN chip set.



Five TMS380 chips form the heart of your LAN adapter. The TMS38030 automatically manages the interface between system memory and the adapter. The TMS38010 processes and buffers data. The TMS38020 contains RAS and LAN-management software and handles data in accordance with IEEE 802.5 protocols. And the TMS38051 and TMS38052 monitor cabling integrity, control network insertion, and perform clocking and signal conditioning.

Q. What about network management?

A. Every service your system needs is built in.

TI's new TMS380 chip set includes "self-healing" features that ensure the reliability, availability, and serviceability (RAS) of the network. And *only* the TMS380 chip set has them.

Among these special features are fault isolation of cable-system failures, error reporting, self-test diagnostics, and LAN-management services. So you're relieved of the risk, time, and expense of developing custom hardware and software for these essential functions.

Q. Can it grow with my needs and my customers'?

A. Yes.

On-chip RAS and LAN-management software make TI's TMS380 chip set completely compatible with the IBM Token-Ring LAN and give it a stable foundation to meet the need for future network expansion. As higher performance standards develop, the TMS380 chip set will accommodate them.

Q. Is training available from Texas Instruments too?

A. Yes.

A three-day workshop on the TMS380 is available at TI's Regional Technology Centers. It includes an introduction to the TMS380 chip set, and hands-on experience in the lab. For information on schedules and reservations, call your TI Field Sales Office or the TI Regional Technology Center nearest you *(list at right).*

Q. Sounds good, but where can I get more details?

A. From your TI Field Sales Office or authorized distributor.

Ask for the TMS380 Product Description.

Q. What's this about an Accelerator Kit?

A. It's your head start to IBM token-ring compatibility.

TI's *Design-in Accelerator Kit* will give you a head start on designing IBM Token-Ring Network compatibility into your products. It includes three chip sets, the *TMS380 User's Guide*, and the *Token Ring Adapter Bring-Up Guide* with debug software. Order yours before March 31 from your nearby TI Field Sales Office or authorized distributor, and get a token good for free admission to TI's three-day TMS380 workshop.

27-5278

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ARIZONA: Phoenix (602) 995-1007; Tucson (602) 624-3276.
CALIFORNIA: Irvine (714) 660-8187; Sacramento (916) 929-1521; San Diego (619) 278-9601; Santa Clara (408) 980-9000; Torrance (213) 217-7010; Woodland Hills (818) 704-7759.
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CANADA: Nepean, Ontario (613) 726-1970; Richmond Hill, Ontario (416) 884-9181; St. Laurent, Quebec (514) 334-3635.

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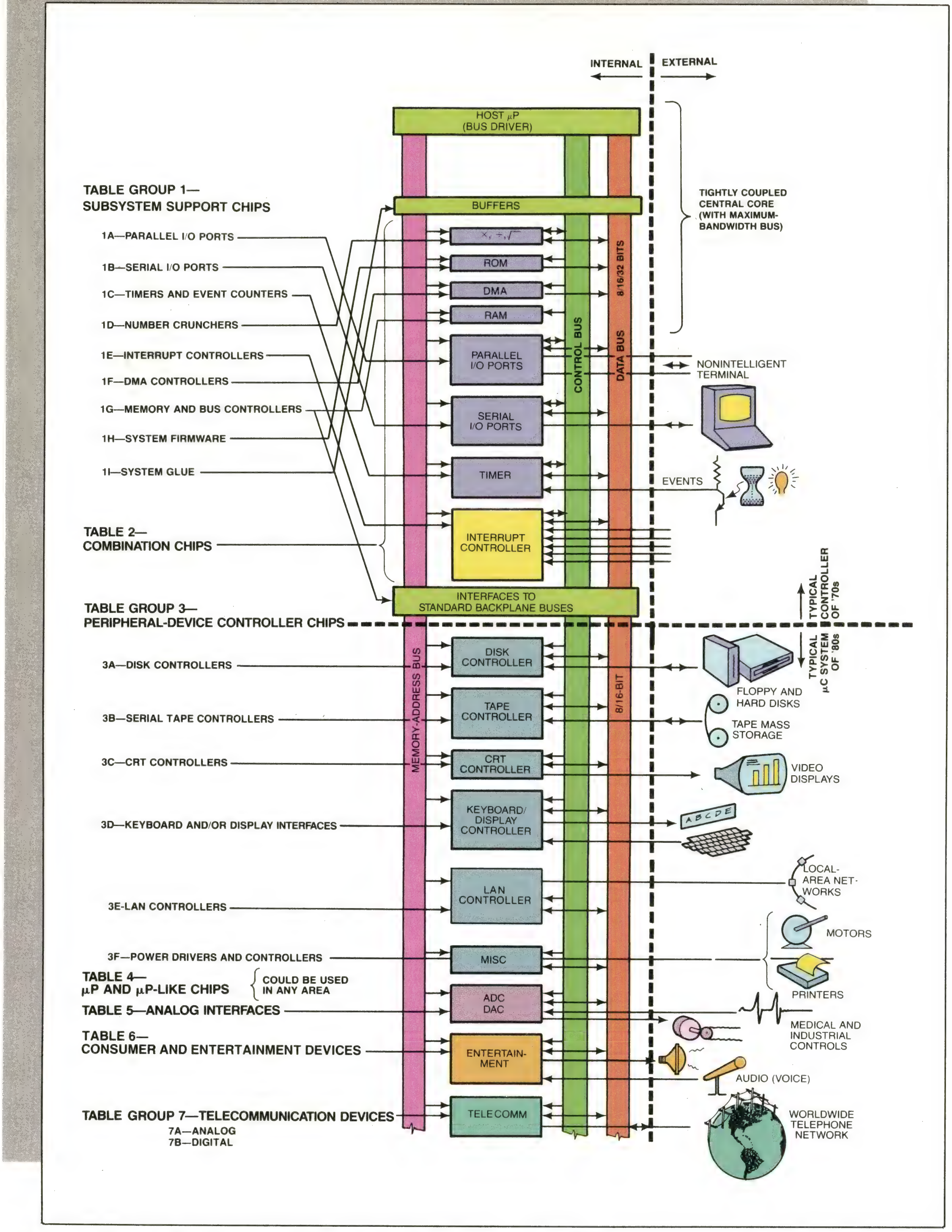

The host µP may be at the top of this µC system, *but it is not necessarily the most important chip in the system. Many of the other support chips listed in this directory, such as number crunchers, slave microcontrollers, ISDN interfaces, and disk, graphics, and LAN controllers, have grown so much in sophistication and performance that they contribute as much, if not more, to overall system performance.*

Support chips mature to upstage the host μP

The availability of CAD megacells and the emergence of ISDN chip sets have combined to enlarge EDN's ninth annual μC Support Chip Directory. This installation gives you a varied representation of the older, standard parts and the newer innovations.

Robert H Cushman, *Special Features Editor*

Two trends in the μP/μC support-chip area have emerged since we published our last directory (EDN, March 7, 1985, pg 138):

- Manufacturers are supplying their chips in standard silicon form or as CAD megacells
- ISDN (Integrated Services Digital Networks) chips sets are nearly complete, and are just waiting for the final standards.

Both of these trends indicate that the μP is no longer the sole, central, glamorous system chip—instead, it's just another component in today's complex products.

The first trend—device suppliers making their designs also available in their semicustom CAD libraries—has made us reevaluate the significance of these chips in our directory. We had thought that, as designers switched from standard products and created their own application-specific ICs on CAD workstations, the need for our directory of standard products would end. But now we see that the directory could evolve into a catalog of the megacells available in semicustom vendors' cell libraries.

VLSI Technology Inc exemplifies the trend of a supplier going the dual route: The company provides devices both as standard parts and as library megacells. If you need a CRT controller, a DMA controller, and a UART, you can either use the company's 68C45, 82C37, and 82C50 separately as standard parts, or you can bring the devices up on your workstation using VLSI's tools for integration into one custom chip. Perhaps today, the 1-chip solution won't turn out to be as completely practical, inexpensive, and dependable in delivery as using the three standard chips off the shelf, but it could be the most appealing approach to designers in the future.

Along with VLSI Technology, other manufacturers—including TRW, NCR, Motorola, Gould/AMI, RCA, and Western Digital—are also working on the dual standard-product/library-megacell approach.

Workstations affect directory listings

The use of CAD workstations is producing a host of new standard parts for our directory. Examples include the LM 628/629 motor controller in **Table 3F**, the PVC-2 video controller in **Table 3C**, and the 32HC01/2/3 memory and I/O interface in **Table 1G**. These devices

Manufacturers are now supplying support chips in two different forms: as standard products and as library megacells.

began as semicustom projects that were later released as standard products. The 628 from National Semiconductor (which received help from SDA Systems Inc, a Santa Clara, CA, software-tools manufacturer) provides sophisticated PID (proportional integral derivative) intelligence for dc motor servo loops. The PVC-2 from Paradise allows color to be simulated in shades of gray on an IBM PC's monochrome monitor. The 32HC01/2/3 interfaces a 32010 digital-signal-processing µP **(Table 4)** to memory and I/O, including codecs. And almost all of the glue parts in **Table 1I** are apt to be the basic entries in CAD cell libraries.

CAD workstations are having an even more direct effect on our directory: Witness the new powerful chips listed in **Table 1D** (number crunching), **Table 1G** (memory and bus management), **Table 3A** (disk controllers), **Table 3C** (CRT controllers), and **Table 3E** (local-area-network controllers). Manufacturers have created many of these devices to answer the performance needs of next-generation CAD workstations.

Major suppliers are ready with ISDN sets

The second trend—the emergence of ISDN chip sets—has prompted us to divide the telecommunications-device section **Table 7** into a digital section (which lists the ISDN sets) and an analog section. In compiling the digital portion, we noticed the µP being connected to a much bigger network, one in which the microprocessor will soon become just another fancy telephone to millions of new users. Use of the ISDN chip sets could spark the beginning of a vast global increase in the use of both µPs and support chips.

ISDN is the standard that will allow the conversion of the international telephone network to completely digital transmission. It represents an enormous market potential because it will use the existing 2-wire loops going to all telephone customers. The conversion has started in areas of Europe where the standards are fully resolved and in a number of trials in the US where the final standard details are still being thrashed out.

In the entries in **Table 7B**, you'll see references to buses labeled "S," "U," and "T1." The S is the new 4-wire bus defined by ISDN for use inside the customer's premise, whether it be a business office or a private home. It's intended to allow economical connection of the multiple devices that would be used in the time-multiplexed ISDN environment—telephones, computer terminals, facsimile printers, etc.

The U bus is the critical portion of ISDN that goes over the existing 2-wire loop between the customer and the telephone company's local central-exchange station. The standards for the U bus have been agreed upon in Europe but not in the US, where the debate is on the hardware and software tradeoffs between having an inexpensive standard that is only suitable for shorter loops (less than two miles), or a more sophisticated and expensive standard that will serve longer loops (more than three miles). At the heart of the issue is the right of, for instance, an isolated farmer in Nebraska to have equal access to a public utility.

The T1, although not directly a part of ISDN, is an existing telephone network trunk. It was originally analog but has been found to be adequate for digital. It can be used to bring higher-capacity digital direct to a customer's PABX.

The opportunities for designers to exploit ISDN will come in several phases. The first, which is already in progress, is to use ISDN techniques in PABX environments. The next step, which should gain momentum in the next few years, will involve applying ISDN to business phones. The final phase will be the gradual extension of ISDN to private consumer phones—a process that could extend well into the next century.

After ISDN is installed, a variety of related markets will open up. New types of codecs will be needed for A/D and D/A conversions in telephones, and computers will need ISDN ports. Imaginative designers will have the opportunity to develop products that take advantage of ISDN capabilitites, such as picture phones matched to ISDN's increased bandwidths and personal-computer equipment and software to take advantage of the user's control over the telephone network with ISDN. **EDN**

Tables begin on pg 123

Article Interest Quotient (Circle One)
High 473 Medium 474 Low 475

Manufacturers of μC support chips

For more information on support chips such as those highlighted in EDN's directory, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card. Abbreviations that conform to those listed in the tables follow some companies' names.

Adaptec Inc
580 Cottonwood Dr
Milpitas, CA 95035
(408) 946-8600
Circle No 606

Advanced Micro Devices (AMD)
901 Thompson Pl
Sunnyvale, CA 94086
(408) 732-2400
Circle No 607

AEG Telefunken
Rte 22, Orr Dr
Somerville, NJ 08876
(201) 722-9800
Circle No 608

Analog Devices
Box 280
Norwood, MA 02062
(617) 329-4700
Circle No 609

Analogic
Audubon Rd
Wakefield, MA 01880
(617) 246-0300
Circle No 610

Beckman Instruments Inc
Advanced Electro Products Div
2500 Harbor Blvd
Fullerton, CA 92634
(714) 773-8126
Circle No 611

Burr-Brown Research Corp
Box 11400
Tucson, AZ 85734
(602) 746-1111
Circle No 612

Cybernetic Micro Systems
Box 3000
San Gregorio, CA 94074
(415) 726-3000
Circle No 613

Dallas Semiconductor
4350 Beltwood Parkway
Dallas, TX 75244
(214) 450-0400
Circle No 614

Data Translation Inc
100 Locke Dr
Marlboro, MA 01752
(617) 481-3700
Circle No 615

Exar Corp
Box 3575
Sunnyvale, CA 94088
(408) 732-7970
Circle No 616

Exel Microelectronics Inc
2150 Commerce Dr
San Jose, CA 95131
(408) 942-0500
Circle No 617

Fairchild (Microprocessors)
450 National Ave
Mountain View, CA 94042
(415) 962-3881
Circle No 618

Fairchild Semiconductor Corp
10400 Ridgeview Ct
Cupertino, CA 95014
(408) 864-6250
Circle No 619

Ferranti Electric Inc
87 Modular Ave
Commack, NY 11725
(516) 543-0200
Circle No 620

Fujitsu
3320 Scott Blvd
Santa Clara, CA 95051
(408) 727-1700
Circle No 621

GE Datel
11 Cabot Blvd
Mansfield, MA 02048
(617) 339-9341
Circle No 622

GE Intersil
10900 N Tantau Ave
Cupertino, CA 95014
(408) 996-5000
Circle No 623

General Instrument Corp (GI)
2355 W Williamsfields Rd
Chandler, AZ 85224
(602) 963-7373
Circle No 624

Gould AMI Semiconductors (G/AMI)
3800 Homestead Rd
Santa Clara, CA 95051
(408) 246-0330
Circle No 625

GTE Microcircuits
2000 W 14th St
Tempe, AZ 85281
(602) 968-4431
Circle No 626

Harris Semiconductor
Box 883
Melbourne, FL 32901
(305) 724-7000
Circle No 627

Hitachi
2210 O'Toole Ave
San Jose, CA 95131
(408) 942-1500
Circle No 628

Hughes Aircraft Co
Solid State Products Div
500 Superior Ave
Newport Beach, CA 92663
(714) 759-2942
Circle No 629

Hunter & Ready Inc
Box 11803
Palo Alto, CA 94306
(415) 326-2950
Circle No 630

Industrial Programming Inc (IPI)
100 Jericho Quadrangle
Jericho, NY 11753
(516) 938-6600
Circle No 631

Integrated Device Technology (IDT)
3236 Scott Blvd
Santa Clara, CA 95051
(408) 727-6116
Circle No 632

International Microcircuits Inc (IMI)
3350 Scott Blvd
Santa Clara, CA 95051
(408) 727-2880
Circle No 633

Intel Corp
2625 Walsh Ave
Santa Clara, CA 95051
(408) 987-8080
Circle No 634

Intel Corp
MCO Marketing
500 W Williams Field Rd
Chandler, AZ 85224
(602) 961-2609
Circle No 635

Intel Corp
3585 SW 198th Ave
Aloha, OR 97007
(503) 681-8080
Circle No 636

ITT Semiconductors
500 Broadway
Lawrence, MA 01841
(617) 688-1881
Circle No 637

JMI Software Consultants Inc
Box 481
Spring House, PA 19477
(215) 628-0846
Circle No 638

LSI Computer Systems Inc
1235 Walt Whitman Rd
Melville, NY 11747
(516) 271-0400
Circle No 639

Micro Networks Inc (Unitrode)
324 Clark St
Worcester, MA 01606
(617) 852-5400
Circle No 640

Mitel Semiconductor
Box 13320
Kanata, Ontario
Canada K2K 1X5
(613) 592-5630
Circle No 641

Monolithic Memories Inc (MMI)
2175 Mission College Blvd
Santa Clara, CA 95054
(408) 970-9700
Circle No 642

Mostek Corp
1215 W Crosby Rd
Carrollton, TX 75006
(214) 466-6000
Circle No 643

Motorola Integrated Circuits
3501 Ed Bluestein Blvd
Austin, TX 78721
(512) 928-6800
Circle No 644

Motorola Semiconductor
5005 E McDowell Rd
Phoenix, AZ 85008
(602) 244-6900
Circle No 645

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 95051
(408) 721-5000
Circle No 646

NCR Microelectronics
2001 Danfield Ct
Fort Collins, CO 80525
(303) 226-9500
Circle No 647

NEC Electronics USA Inc
NEC Microcomputer Div
1 Natick Executive Park
Natick, MA 01760
(617) 655-8833
Circle No 648

Oki Semiconductor Inc (OKI)
650 N Mary Ave
Sunnyvale, CA 94086
(408) 720-1900
Circle No 649

Pacific Microcircuits Ltd
1645 140th St
White Rock, British Columbia
Canada V4A 4H1
(604) 536-1886
Circle No 650

Panasonic Co
Electronic Components Div
1 Panasonic Way
Secaucus, NJ 07094
(201) 348-5270
Circle No 651

Paradise Systems Inc
217 E Grand Ave
South San Francisco, CA 94080
(415) 588-6000
Circle No 652

Plessey Semiconductors Inc
1641 Kaiser Ave
Irvine, CA 92714
(714) 540-9979
Circle No 653

Precision Monolithics Inc (PMI)
1500 Space Park Dr
Santa Clara, CA 95050
(408) 246-9222
Circle No 654

RCA Solid State Div
Rte 202
Somerville, NJ 08876
(800) 526-2177
Circle No 655

Rockwell International Corp
Semiconductor Div
Box C
Newport Beach, CA 92660
(714) 833-4700
Circle No 656

SGS/ATES Semiconductor Corp
1000 E Bell Rd
Phoenix, AZ 85002
(602) 867-6100
Circle No 657

Seeq Technology Inc
1849 Technology Dr
San Jose, CA 95131
(408) 262-5041
Circle No 658

Sharp Electronics Corp
10 Keystone Pl
Paramus, NJ 07652
(201) 265-5600
Circle No 659

Siemens Corp
186 Wood Ave S
Iselin, NJ 08830
(201) 494-1000
Circle No 660

Signetics
811 E Arques Ave
Sunnyvale, CA 94086
(408) 739-7700
Circle No 661

Siliconix Inc
2201 Laurelwood Rd
Santa Clara, CA 95054
(408) 988-8000
Circle No 662

Solid State Scientific Inc (SSS)
Commerce Dr
Montgomeryville, PA 18936
(215) 657-8400
Circle No 663

Sprague Electric Co
115 NE Cutoff
Worcester, MA 01606
(617) 853-5000
Circle No 664

Standard Microsystems Corp (SMC)
35 Marcus Blvd
Hauppauge, NY 11787
(516) 273-3100
Circle No 665

Supertex Inc
1225 Bordeau Dr
Sunnyvale, CA 94086
(408) 744-0100
Circle No 666

Teledyne Semiconductor
1300 Terra Bella Ave
Mountain View, CA 94043
(415) 968-9241
Circle No 667

Teltone Corp
Box 657
Kirkland, WA 98033
(206) 827-9626
Circle No 668

Texas Instruments Inc (TI)
Microfunctions
13536 N Central Expressway
Dallas, TX 75265
(214) 995-3637
Circle No 669

Texas Instruments Inc (TI)
MOS Microcomputers
9901 S Wilcrest Dr
Houston, TX 77099
(713) 879-2000
Circle No 670

Thomson Components—
Mostek Corp (Mostek)
1310 Electronics Dr
Carrollton, TX 75006
(214) 466-6000
Circle No 671

Toshiba America Inc
2692 Dow Ave
Tustin, CA 92680
(714) 823-6300
Circle No 672

TRW/LSI Products
Box 2472
La Jolla, CA 92038
(619) 457-1000
Circle No 673

VLSI Technology Inc (VTI)
10220 S 51 St
Phoenix, AZ 85044
(602) 893-0807
Circle No 674

Weitek Corp
1060 E Arques Ave
Sunnyvale, CA 94086
(408) 738-8400
Circle No 675

Western Design Center (WDC)
2166 E Brown Rd
Mesa, AZ 92714
(602) 962-4545
Circle No 676

Western Digital (WD)
2455 McCabe Way
Irvine, CA 95008
(714) 863-0102
Circle No 677

Zilog Inc
1315 Dell Ave
Campbell, CA 95008
(408) 730-8000
Circle No 678

Zymos Corp
Box 62379
Sunnyvale, CA 94088
(408) 730-8800
Circle No 679

Zytrex Corp
224 N Wolfe Rd
Sunnyvale, CA 94086
(408) 733-3973
Circle No 680

TABLE GROUP 1—SUBSYSTEM SUPPORT CHIPS

1A PARALLEL I/O PORTS

TYPICALLY HAVE AT LEAST TWO 8-BIT PORTS WITH LATCHES AND TWO HANDSHAKING LINES PER PORT FOR INTERFACING TO PERIPHERALS. IN SOME DEVICES, THE HOST µP CAN USE INTERNAL CONTROL REGISTERS TO SET UP BIT LINES AS INPUTS OR OUTPUTS.

µP BUS COMPAT-IBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS				TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
				PORT 1 BITS	PORT 2 BITS	PORT 3 BITS	PORT 4 BITS			
8080/85 8086/88 NSC800 70008	HARRIS INTEL, OKI INTERSIL NEC	82C55A PPI 71055	5 MHz 8 MHz	8	8	4	4	CMOS +5V 40-PIN PLCC	\$4.67 \$5.50 NOW NOW \$14.65	4-BIT PORTS CAN PROVIDE HAND-SHAKE FOR 8-BIT PORTS. CMOS REPLACEMENT FOR NMOS 8255A. NEC 71055 IS EQUIVALENT
6800 6809 6502	MOTOROLA HITACHI ROCKWELL	6821 6321 65C21	2 MHz 4 MHz	8+2 HAND-SHAKE	8+2 HAND-SHAKE	—	—	NMOS 40-PIN CMOS 40-PIN 54-PIN FLAT PACK	\$2.05 NOW \$3.35 NOW	BASIC PIA, NOW ALSO WIDELY AVAILABLE IN CMOS
68HC11	MOTOROLA	68HC24	2.1 MHz	8+1 HAND-SHAKE	8+1 HAND-SHAKE	—	—	HMOS 44-PIN SURFACE MOUNT 40-PIN	\$18.40 NOW	68HC24 IS COMMONLY USED AS A PORT REPLACEMENT WHEN 68HC11 IS USED AS µP. MAKES UP FOR PORTS LOST
6502	ROCKWELL	65C24	4 MHz	8+2 HAND-SHAKE	8+2 HAND-SHAKE	—	—	CMOS 40-PIN	\$3.80 NOW	ALSO CONTAINS 1 x 16-BIT COUNTER
146805E2 146805E3 6801 6803	MOTOROLA	146823	1 MHz	8	8	8	—	CMOS 40-PIN 44-PIN PLCC	\$4.05 NOW	PIN PROGRAMMABLE TO ALSO SUIT INTEL µPs ("MOTEL" INTERFACE)
68000	MOTOROLA	68230	8, 10 MHz	8/16	8/16	8/16	24-BIT PROGRAM TIMER	HMOS +5V 48-PIN	\$6.64 NOW	INTERRUPT LOGIC & PROGRAM-MABLE HANDSHAKING
µPD70008 8080/85 8086/88	NEC	71055 7210	8 MHz	—	—	—	—	NMOS +5V 40-PIN	\$4.67 \$14.65 NOW	GPIB (IEEE-488) TALKER & LIS-TENER, CONTROLLER CHIP SET
GENERAL	SMC	COM 7210	8 MHz	IEEE-488	—	—	—	NMOS +5V 40-PIN	\$16 NOW	SIMILAR TO NEC 7210. TALKER/LISTENER/CONTROL
GENERAL	TI	9914A	5 MHz	8, +8 HAND-SHAKE	—	—	—	NMOS +5V 40-PIN	\$21 NOW	IEEE-488 LISTENER/TALKER CONTROLLER WITH COMPLETE CONTROL BUS
GENERAL 8, EXPAND-ABLE TO 16, 32	TI	9650 MPIF	3.7M BYTES/SEC	8+ CON-TROL LINES	8+ CON-TROL LINES	—	—	NMOS +5V 40-PIN	\$15 NOW	A MEANS FOR ASYNCHRONOUSLY LINKING TWO µPs TOGETHER WITH 256-BYTE RAM BUFFER BETWEEN
Z80	TOSHIBA ZILOG	Z80C PIO, Z84C20	DC-4, 6-MHz µP CLOCK	8+2 HAND-SHAKE	8+2 HAND-SHAKE	—	—	CMOS +5V 40-PIN 44-PIN FP	\$2.40 NOW	CMOS VERSION OF NMOS Z8420 & Z8320. 2 mA AT 4 MHz AND LESS THAN 10 µA AT 5V POWER DOWN (CLOCK STOPPED)
Z8000 80860 6800	ZILOG	Z8536 Z8036	4, 6 MHz	8	8	4	—	NMOS +5V 40-PIN	\$5 NOW	BIT PORT HANDSHAKING. 8536 MATCHES 8086 BUS. 8036 MATCHES 6800 BUS

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

1B SERIAL I/O PORTS

ORIGINALLY USED MAINLY FOR SIMPLE ASYNCHRONOUS TELETYPE CONTROL, THESE DEVICES NOW SERVICE AN INCREASING NUMBER OF COMPLEX SYN-CHRONOUS PROTOCOLS. THIS DIRECTORY ALSO LISTS SOME VERY SIMPLE 3-WIRE SERIAL PORTS FOR SMALL SYSTEMS **(TABLE 4)** AND SOME SOPHISTICATED INTERFACES TO NETWORKS **(TABLE 3E)**.

µP BUS COMPAT-IBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS				TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
				SDLC	HDLC	ADCCP	BISYNC			
8080/85 8086/88 NSC800 70008	INTEL OKI NEC	82C51 71051	64k BPS SYNCH, 38.4k BPS ASYNCH	—	—	—	—	CMOS +5V 28-PIN	\$5.40 NOW \$5.69	CMOS VERSION OF INTEL 8251 USART. PROGRAMMABLE BAUD RATE. ERROR DETECTION
8080/85 8086/88 NSC800 70008	NEC	7201A	1.25M BPS	YES	YES	YES	YES	NMOS +5V 40-PIN	\$14 NOW	FASTER VERSION OF 7201, 8274
GENERAL (10 BITS)	NATIONAL	DP 8340 DP 8341	3.5M BPS (28-MHz CLOCK)	— —	— —	— —	— —	BIPOLAR LOW-POWER SCHOTTKY 24-PIN 28-PIN PCC	\$40 PER SET NOW	ENCODER/DECODER PAIR MEET IBM 3270 BIPHASE INFORMATION DISPLAY STANDARD AT 2.3587M BPS
GENERAL (8 BITS)	NATIONAL	DP 8342 DP 8343	3.5M BPS (28-MHz CLOCK)	— —	— —	— —	— —	BIPOLAR LOW-POWER SCHOTTKY 24-PIN 28-PIN PCC	\$30 PER SET NOW	GENERAL-PURPOSE HIGH-SPEED MANCHESTER ENCODER/DECODER PAIR
GENERAL (8 BITS)	NATIONAL VTI WEST DIG HARRIS	82C50 82C50A 16C450 16550	0–1.5M BPS+	YES	YES	YES	YES	CMOS +5V 40-PIN 44-PIN PLCC	\$8.44 NOW \$16.32	DUAL MULTIPROTOCOL ASYN-CHRONOUS FOR SERIAL DATA TO MODEMS, TAPE & DISK DRIVES

1B SERIAL I/O PORTS *(continued)*

µP BUS COMPAT-IBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS SDLC	HDLC	ADCCP	BISYNC	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	NATIONAL	DS 14C88 14C89A	—	—	—	—	—	CMOS +5V 14-PIN 14-PIN SO	$1.30 NOW	RS-232C DRIVER/RECEIVER CMOS-COMPATIBLE VERSION OF CLASSIC BIPOLAR 1488. LOWER POWER. NO NEED FOR PULSE-SHAPING CAPs
6500	ROCKWELL GTE, WDC RCA, MITEL G/AMI	65C51 ACIA	1–4 MHz	—	—	—	—	CMOS +5V 28-PIN SURFACE MOUNT	$4 NOW	CMOS REPLACEMENT FOR NMOS 6551. SURFACE-MOUNT PKG FROM G/AMI
6500	ROCKWELL	65C52	1–4 MHz	—	—	—	—	CMOS 40-PIN	$8.50 NOW	DUAL ACIA (65C51) WITH DUAL BAUD-RATE GENERATOR
6805 8085 8086/88 NSC800	RCA	6853	2 MHz (50–19.2k BAUD)	—	—	—	—	CMOS +5V 28-PIN	$7.95 NOW	MULTIPLEXED BUS VERSION OF 65C51
6800 6809	MOTOROLA	6850	1.5 MHz	—	—	—	—	NMOS 24-PIN	$2.20 NOW	IM-BPS TRANSFER RATE
6800 6809	MOTOROLA	6852	1.5 MHz	—	—	—	—	NMOS 24-PIN	$3.35 NOW	
6800 6809	MOTOROLA	6854	1.5 MHz	YES	YES	YES	—	NMOS 28-PIN	$5 NOW	
68000	MOTOROLA	68605 XPC	10, 12.5 MHz	YES	YES	—	YES	HCMOS 84-PIN PGA	$68.75 NOW	IMPLEMENTS 1984 CCITT X.25 LAPB. GENERATES LINK LEVEL COMMAND & RESPONSES. ON-CHIP DMA
68000 6800	ROCKWELL	68561 MPCC 68560	8 MHz (BIT RATE WITH CRC)	YES	YES	YES	YES	NMOS +5V 48-PIN 40-PIN	$33.75 NOW $30.40 NOW	68561 SUPPORTS 16-BIT OPERATION WHEN CONNECTED TO 68000 BUS. 4M BPS MAX DATA -TRANSFER RATE. BAUDOT, X.25 ETC
68000	SIGNETICS MOTOROLA	68652 (2652) MPCC	2M BPS	YES	YES	YES	YES	NMOS +5V 40-PIN	$5.80 NOW	SELF-TEST MODE, ERROR CON-TROL, FULL/HALF DUPLEX
68000	SIGNETICS MOTOROLA INTERSIL	68661 (2661) EPCI 26c61	0–1M BPS	—	—	—	YES	NMOS +5V 28-PIN CMOS +5V	$3.50 NOW 1Q86	INTERNAL BAUD-RATE GENERATOR, DOUBLE-BUFFERED RECEIVE/TRANSMIT. SYNCH OR ASYNCH
68000	SIGNETICS MOTOROLA	68681 (2681) DUART	1M BPS	—	—	—	—	HMOS +5V 40-PIN 28-PIN 24-PIN	$4.50 NOW	TWO INDEPENDENT FULL DUPLEX CHANNELS. QUADRUPLE BUFFERED RECEIVERS
GENERAL	SIGNETICS	2641	DC-1 MHz	—	—	—	—	NMOS +5V 24-PIN	$2 NOW	UART WITH ADVANCED FEATURES SUCH AS DIAGNOSTICS. SIMILAR TO 2661
68000	SIGNETICS	68562 DUSCC	4M BAUD	YES	YES	YES	YES	NMOS +5V 40-PIN	NA NOW	BAUD-RATE GENERATORS, DPLL, DUAL CHANNEL, FULL DUPLEX, DATA ENCODING, MULTIPROTOCOL
GENERAL	SIGNETICS	2691	1M BPS (50–38.4k BAUD)	—	—	—	—	CMOS +5V 24-PIN	$5 NOW	SIMILAR TO 2681
GENERAL	SIGNETICS	2698	1M BPS (50–38.4k BAUD)	—	—	—	—	CMOS +5V 48-PIN 84-PIN	$30 2H86	OCTAL UART (8 UARTS) PLUS 4 MULTIFUNCTION 16-BIT COUN-TER/TIMERS
GENERAL	SMC	8017	DC-40k BAUD	—	—	—	—	NMOS +5V 40-PIN	$4.60 NOW	NMOS VERSION OF 2017. SAID TO BE A CLASSIC UART
GENERAL	SMC	COM 9004	2.35M BPS	—	—	—	—	NMOS +5, +12V 40-PIN	$20.95 NOW	IBM 3274/76/78 RECEIVER/TRANSMITTER, MANCHESTER ENCODE/DECODE ON CHIP, 20-MHz CLOCK
Z80	TOSHIBA ZILOG	Z80C SIO Z84C40 /41/42	DC-4 MHz, 800k BAUD	YES	YES	—	YES	CMOS +5V 40-PIN 44-PIN FLAT PACK	$9.05 NOW	CMOS VERSION OF NMOS Z844X & Z834X. 1/10TH OPERATING POWER & LESS THAN 10 µA WHEN POWERED DOWN (CLOCK STOPPED). ALSO ASYNCHRONOUS
Z8000	ZILOG AMD SGS	Z8530 SCC Z8030	4, 6, 10 MHz	YES	YES	—	YES	NMOS +5V 40-PIN	$6.95 NOW	OSCILLATOR & BAUD-RATE GENER-ATOR. SAID TO BE AN INDUSTRY STANDARD
Z8000	ZILOG TOSHIBA SGS	Z8031 Z8531 ASCC	4, 6, 10 MHz	—	—	—	—	NMOS +5V 40-PIN 44-PIN	$8.59 NOW	PROGRAMMABLE FOR FM, NRZ & NRZI
8086 Z80 68000	EXEL	88C681 68C681 DUART	NA	—	—	—	—	CMOS 40-PIN 28-PIN 40-PIN 44-PIN PLCC	$8.30 NOW	CMOS VERSION OF 2681 DUART (SIGNETICS)
8086 Z80 68000	EXEL	88C565 68C565	NA	YES	YES	YES	—	CMOS 48-PIN	NA 1987?	BIT ORIENTED, COPROCESSOR ARCHITECTURE TO UNLOAD HOST µP. (FINANCIAL PROBLEMS OF EXEL DELAYING INTRODUCTION)

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

1240 and 1630 were fine,

but this is 1986.

Back in the days when logic analysis alone was enough to test your designs, Tek's 1240* or HP's 1630** served you well.

But nowadays, your designs are more sophisticated and complex, combining microprocessors, ASICs, and discrete logic. And you're doing your software development in high-level and assembly language. So you need more than just logic analysis. You need a modular analysis system: the μAnalyst from Northwest Instrument Systems.

With the μAnalyst, high-performance state and timing analysis are only the beginning. Our Interactive Pattern Generator easily simulates outputs from even the most complex components. Or you can stimulate the inputs to your prototype system and analyze the results.

And our SoftAnalyst is the only system designed for the special problems of analyzing high-level language software. Now you can trace your software's real-time execution, analyze its performance, and make sure you've exhaustively tested your code—all in the high-level language you wrote it in.

	Tek 1240	HP 1630G	NWIS μAnalyst
State Logic Analysis	Yes	Yes	Yes
Channels	36	57	80
Trigger Levels	14	5	15
Memory Depth	2K	1K	4K
State/Timing Correlation/ Display	No	No	Yes
Timing Logic Analysis	Yes	Yes	Yes
Acquisition Speed	100MHz	100MHz	100MHz
Channels	18	8	16
Transitional Timing	No	No	Yes
Pattern Generation	No	No	Yes
Channels	-	-	160
Speed	-	-	20MHz
Vector Depth	-	-	8K
Software Analysis	assembly only	assembly only	high-level and assembly
Symbolic Trace	No	No	Yes
Performance Analysis	statistical	statistical	real-time non-statistical
Code Coverage	No	No	Yes

1240 includes 2-1240D1 & 2-1240D2 - 1630G includes 57 state/8 timing
NWIS μAnalyst includes 80 state/16 timing

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Circle 11 for Literature

Circle 50 for Demonstration

THE ONLY QUICK–TURN GUARANTEE.

Feature Size: 2μ

	N-Channel	P-Channel
VTEO	0.5–1.0$_V$	0.5–1.0$_V$
BVDSS	>10$_V$	>10$_V$
$K^1 = \frac{\mu c}{2}$ linear region	21–25	6.5—8.5
B_E(Long Channel)	0.8–1.2$_V{}^{1/2}$	0.4—0.6$_V{}^{1/2}$
Cap. Gate 10^4 PF/cm^2	8–10	8–10
Cap. Poly to Sub 10^4 PF/cm^2	0.55–0.65	0.55–0.65
Cap. Metal to Sub 10^4 PF/cm^2	0.27–0.32	0.27–0.32
Junction Depth	0.4μ–0.6μ	0.2μ–0.4μ
P-Well Junction	2.5μ–3.5μ	
Poly P_S	15–30Ω/□	15–30Ω/□
Diffusion P_S	20–40Ω/□	60–100Ω/□
VTF Poly	>10$_V$	>10$_V$
ΔW	—1.0μ	—1.2μ
LEFF	1.0μ–1.4μ	1.3μ–1.7μ
Substrate Resistivity	2.5KΩ/□	1.2Ω/cm

Feature Size: 3μ

	N-Channel	P-Channel
VTEO	0.5-1.0$_V$	0.5–1.0$_V$
BVDSS	>10$_V$	>10$_V$
$K^1 = \frac{\mu c}{2}$ linear region	18–21	6–8
B_E(Long Channel)	0.8–1.4$_V{}^{1/2}$	0.4—0.6$_V{}^{1/2}$
Cap. Gate 10^4 PF/cm^2	5.9–7.0	5.9– 7.0
Cap. Poly to Sub 10^4 PF/cm^2	0.45–0.55	0.45–0.55
Cap. Metal to Sub 10^4 PF/cm^2	0.2–0.25	0.2–0.25
Junction Depth	0.6μ–1.0μ	0.4μ–0.8μ
P-Well Junction	3.5μ–4.5μ	
Poly P_S	15–30Ω/□	15–30Ω/□
Diffusion P_S	10–30Ω/□	30–70Ω/□
VTF Poly	>10$_V$	>10$_V$
ΔW	—1.0μ	—1.0μ
LEFF	1.4μ–2.0μ	1.8μ–2.4μ
Substrate Resistivity	2.5KΩ/□	1.0–1.5Ω/cm

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STILL

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CIRCLE NO 118

1C TIMERS AND EVENT COUNTERS

PROVIDE ONE OR MORE UP- OR DOWN-COUNTING REGISTERS THAT CAN BE PRESET VIA PROGRAM CONTROL BY µP AND THEN COUNT OUT CLOCK CYCLES AND FLAG µP BY INTERRUPT WHEN DONE. SOME COUNT PULSES (EVENTS) ON INPUT LINE. ALSO INCLUDED ARE OTHER TIMING FUNCTIONS SUCH AS SYSTEM CLOCKS AND REAL-TIME CLOCKS.

µP BUS COMPAT-IBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS				TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
				TIMER 1 BITS	TIMER 2 BITS	TIMER 3 BITS	TIMER 4 BITS			
6800 6809	MOTOROLA HITACHI	6840 6340	2 MHz (4, 8 MHz)	16	16	16	—	NMOS CMOS 28-PIN	$4.45 NOW	PROGRAMMABLE SO TIMERS CAN BE USED FOR MANY DIFFERENT TASKS
146805E2 146805E3	MOTOROLA HITACHI	146818A	1 MHz	—	—	—	—	CMOS 24-PIN FLAT PACK 44-PIN PLCC	$4.65 NOW	REAL-TIME CLOCK/CALENDAR WITH 64 BYTES RAM (50 GENERAL PURPOSE). AN INDUSTRY STANDARD
68HC05 D2/D4	RCA	68HC 68T1	(SPI)	—	—	—	—	CMOS 16-PIN	$4.70 2Q86	REAL-TIME CLOCK WITH TIME/CALENDAR, 32-BYTE RAM & 3-WIRE "SPI" BUS
80286	INTEL AMD	82284	6, 8, 10 MHz	—	—	—	—	BIPOLAR 18-PIN	$14.70 NOW	CLOCK GENERATOR/DRIVER PROVIDES CLOCK, READY & RESET SIGNALS FOR 80286
GENERAL	AMD	9513A	NA	16	16	16	2 x 16	NMOS +5V 40-PIN	$19.90 NOW	HAS FIVE TIMERS
3200	TI	32201 TCU	10 MHz	—	—	—	—	BIPOLAR 24-PIN	$5 NOW	WAIT-STATE GENERATOR. CYCLE HOLD FOR SLOW PERIPHERALS
8080/85 8086/88 NSC800 70008	OKI INTERSIL	82C53	5 MHz	16	16	16	—	CMOS +5V 24-PIN	$4–$5 NOW	TIMER, CMOS VERSION OF INTEL NMOS 8283. HAS 6 COUNTER MODES, BINARY & DECIMAL
8080/85 8086/88 +SC800 70008	HARRIS OKI, VTI INTERSIL NEC	82C54 71054	DC-10 MHz COUNT RATE	16	16	16	—	CMOS +5V 24-PIN	$5–$9 NOW	TIMER, COMPATIBLE WITH INTEL NMOS 8254 AND SUPERSET OF NMOS/CMOS 8283/83C83
80C86/88	HARRIS INTEL OKI VTI	82C84 82C84A	DC-8 MHz (0-25 MHz OSC)	—	—	—	—	CMOS +5V 18-PIN	$3.67 NOW	CLOCK GENERATOR FOR 80C86/88 WITH RESET & READY SYNCHRONIZATION
80C86 80C88	HARRIS	82C85	DC-8 MHz	—	—	—	—	CMOS +5V 24-PIN SLIMLINE	$7.95 NOW	SUPERSET OF 82C84A CLOCK GENERATOR. 4 CLOCK FREQ MODES FOR LOW-POWER STATIC CMOS DESIGNS
GENERAL	OKI	6242	280-nSEC ACCESS	—	—	—	—	CMOS 18-PIN	$4 NOW	REAL-TIME CLOCK, WITH POWER-FAIL DETECT, DEDICATED I/O & ADDRESS. BUS NIBBLE
GENERAL	INTERSIL	7170	300-nSEC ACCESS	—	—	—	—	CMOS +5V 24-PIN	$4 NOW	REAL-TIME CLOCK, 100 SEC TO 99 YEARS, 2-µA STAND-BY, 4 CRYSTAL FREQ, PERIODIC & ALARM INTERRUPTS, CALENDAR, MIL TEMP, ON-CHIP BATTERY BACKUP
Z80	ZILOG	Z8581	20 MHz	—	—	—	—	NMOS +5V 18-PIN	$3.50 NOW	CLOCK OSCILLATOR & CONTROLLER INTENDED FOR Z80 BUT SAID TO BE USEFUL FOR OTHER µPs
Z80	TOSHIBA	T6497	NA	—	—	—	—	CMOS +5V 16-PIN	$1.50 NOW	CMOS CLOCK FOR CMOS Z80. HAS INPUTS THAT COMMAND RUN, IDLE, & STOP TO SAVE POWER
Z80	TOSHIBA ZILOG	Z80C CTC Z84C30	DC-4 MHz	16	16	16	16	CMOS +5V 40-PIN 44-PIN FLAT PACK	$2.40 NOW NOW	CMOS VERSION OF NMOS Z8430 & Z8330. 1/10TH OPERATING POWER & LESS THAN 10 µA WHEN POWERED DOWN (CLOCK STOPPED)
Z80	ZILOG	Z84C60	4 MHz	16	16	16	16	CMOS +5V 40-PIN	$2.55 NOW	CLOCK GENERATOR/TIMER (−40 TO +85°C) RUN, IDLE, STOP COMMANDS TO SAVE POWER
GENERAL	LSI COMPUTER SYSTEMS	7066	DC-5 MHz	24	—	—	—	NMOS 20-PIN	$7.10 NOW	HOST µP CAN SET UP BINARY, BCD, 24-HOUR CLOCK, UP/DOWN, DIVIDE-BY-N, QUADRATURE & SINGLE CYCLE MODES

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

1D NUMBER CRUNCHERS

PROVIDE HARDWIRED OR FIRMWARE IMPLEMENTATION OF DATA-MANIPULATION INSTRUCTIONS THAT ARE OTHERWISE DIFFICULT TO PROGRAM AND SLOW TO ACCOMPLISH WITH MAIN µP. INCLUDES INTEGER AND FLOATING-POINT MULTIPLICATION, TRIG FUNCTIONS, AND SPECIAL ALGORITHMS SUCH AS ENCRYPTION. SEE ALSO **TABLE 3C** FOR GRAPHIC ALGORITHMS.

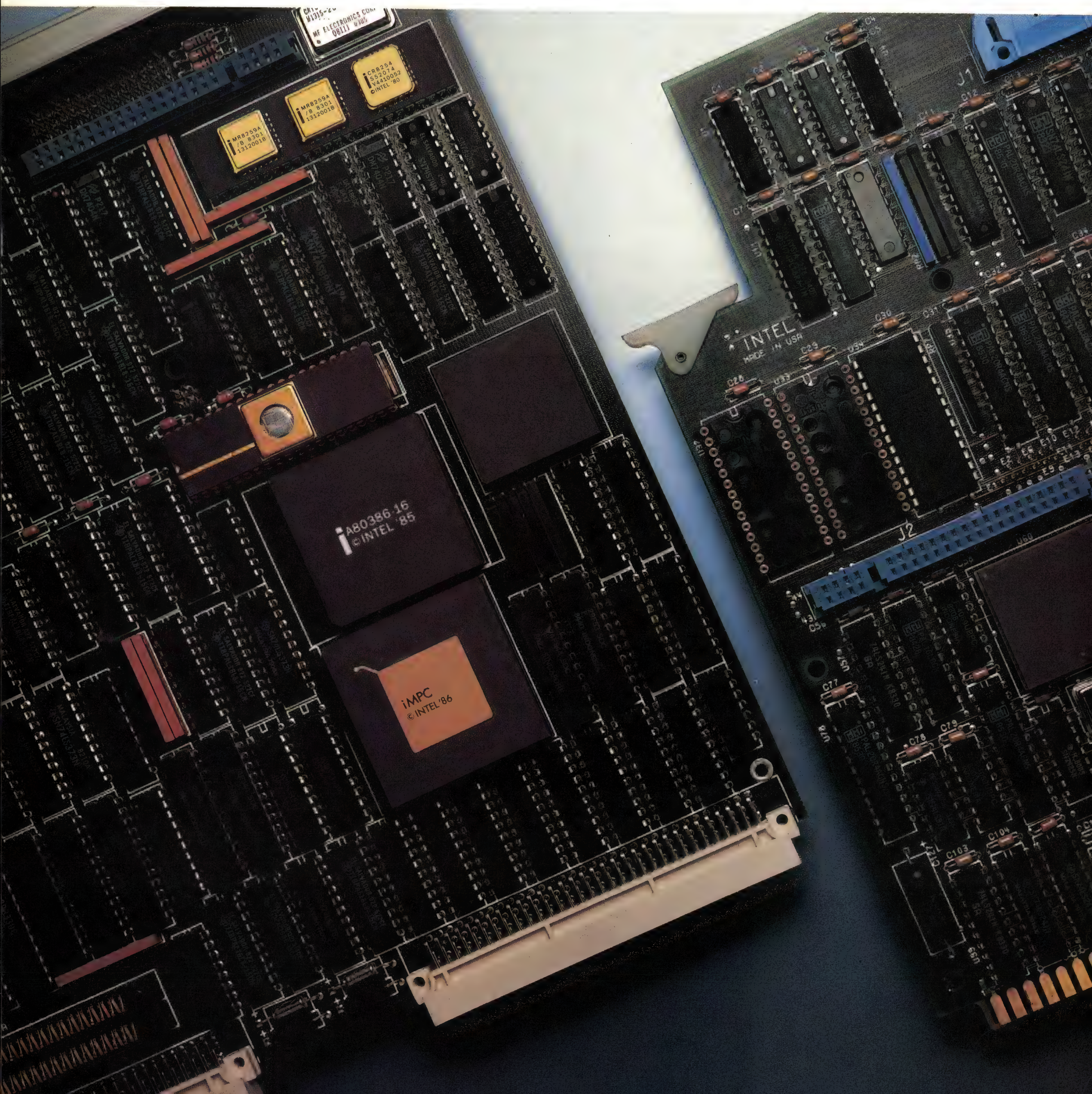
µP BUS COMPAT-IBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS			TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
				MATH	TRIG	FL PT			
GENERAL	ANALOG DEVICES	ADSP 1009A	75 nSEC	12 x 12	NO	NO	CMOS 64-PIN	$75 1Q86	HIGH-SPEED, LOW-POWER (200-mW) REPLACEMENT TDC-1009J
GENERAL	ANALOG DEVICES	ADSP 1080A	45 nSEC	8 x 8	NO	NO	CMOS 40-PIN	$64 1Q86	HIGH-SPEED, LOW-POWER (175-mW) REPLACEMENT FOR TDC-8HJ

1D NUMBER CRUNCHERS *(continued)*

µP BUS COMPATIBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS MATH	TRIG	FL PT	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	ANALOG DEVICES	ADSP 1012A	55 nSEC	12 x 12	NO	NO	CMOS 64-PIN	$27 1Q86	HIGH-SPEED, LOW-POWER (300-mW) REPLACEMENT FOR MPY-12HT
GENERAL (BIT & WORD SLICE)	ANALOG DEVICES	ADSP 3210 3220	10 MHz (10M FLOPS)	x, −	—	YES	CMOS +5V 100-PIN PGA 144-PIN PGA	$350 NOW	IEEE 754 (DRAFT 10.0) FOR 32- & 64-BIT FLOATING POINT. CHIP SET DOES FP MULT, ADD IN 100 nSEC AT 400 mW/CHIP
GENERAL	TI	1010-100 1010-140	100 nSEC 140 nSEC	16 x 16, +, −	—	—	CMOS +5V 64-PIN	$92 $75 NOW	150-mW POWER CONSUMPTION. COMPATIBLE WITH TDC1010
GENERAL	TI	29516	85 nSEC	x, +, −	—	—	CMOS +5V 64-PIN	NA 1Q86	LOW POWER, COMPATIBLE WITH Am29516
GENERAL	TI	29517	85 nSEC	x, +, −	—	—	CMOS +5V 64-PIN	NA 1Q86	LOW POWER, COMPATIBLE WITH Am29517
GENERAL	TI	1010A-60	60 nSEC	16 x 16, +, −	—	—	CMOS +5V 64-PIN	NA 1Q86	60-nSEC VERSION OF THCT1010
GENERAL	TI	29116 29117	NA	+, −, LOGICAL OPERATIONS, SHIFT, ROTATE	—	—	CMOS +5V 52-PIN 68-PIN	NA 1Q86	16-BIT MICROPROGRAMMABLE CONTROLLER
GENERAL	TI	ACT 8836	80 nSEC	32 x 32, +, −	—	—	CMOS +5V, (1 µm) 156-PIN	NA 3Q86	32-BIT MULT/ACCUM, CAN PERFORM 64 x 64 FUNCTIONS, ACCUM. BYPASS, OVERFLOW STATUS, PARITY GEN/CHECK, MASTER/SLAVE CIRCUITRY
GENERAL	TI	ACT 8837	80 nSEC	+, −, x, ÷	—	YES 32- & 64-BIT IEEE	CMOS +5V (1 µm) 156-PIN	NA 3Q86	MULT & ALU IN ONE CHIP. FLT PT TO INTEGER & VICE VERSA CONVERSION, PIPELINED OR FLOWTHROUGH
GENERAL (16-BIT)	NCR	45CM16	220 nSEC	16 x 16	NO	NO	CMOS +5V 24-PIN	$42.90 NOW	ASYNCHRONOUS SINGLE-PORT PARALLEL MULT/ACCUM
GENERAL (1-BIT)	NCR	74HCT384	20 MHz	N x 8	NO	NO	CMOS +5V 16-PIN	$4.35 NOW	BIT-SERIAL MULTIPLIER
GENERAL (1-BIT)	NCR	74HCT784	20 MHz	N x 8	NO	NO	CMOS +5V 20-PIN	$5.17 NOW	74HCT384 PLUS ADDER/SUBTRACTOR
GENERAL (4-BIT)	NCR	74HCT-784 x 4	20 MHz	N x 8	NO	NO	CMOS +5V 68-PIN	$16.54 NOW	MONOLITHIC QUAD VERSION OF 74HCT784
GENERAL	NCR	45CG72 (GAPP)	10 MHz	+, − LOGICALS	NO	NO	CMOS 74-PIN PGA	$395 NOW	SYSTOLIC ARRAY BUILDING BLOCK CONTAINING 72 BIT-SERIAL PROCESSORS. CASCADABLE IN 2 DIMENSIONS
GENERAL	AMD	7970 CEP	2M BPS 5 MHz	—	—	—	NMOS 68-PIN LCC	$240 NOW	DATA COMPRESSOR. SAID TO COMPRESS DATA ON 8½ x 11-IN. PAGE UP TO 50X IN 1–2 SEC
29300 29400	AMD	29325	8 MHz (125-nSEC INSTR CYCLE)	x, +, −	NO	YES	BIPOLAR 144-PIN	$695 NOW	IEEE & DEC COMPATIBLE WITH CONVERSION BETWEEN. SAID TO AVOID "TOO MUCH" PIPELINING SO FASTER FOR GENERAL-PURPOSE USE
GENERAL	VTI	16160	(4 TIMES FASTER THAN SOFTWARE)	AND OR XOR SHIFT	NO	NO	CMOS 28-PIN	$16.03 NOW	INTENDED AS HARDWARE ASSIST FOR BIT-MAPPED GRAPHICS. HAS 32-BIT BARREL SHIFTER & BOOLEAN ALU
GENERAL	VTI	2010 2044	50 nSEC (TYP)	16 x 16, +	NO	NO	CMOS 64-PIN PLCC	$32.54 $38.51	MULTIPLY ACCUMULATORS. SIMILAR TO INDUSTRY-STD 1010 TYPES, BUT 2044 HAS NO PRELOAD
80286 (16 BITS) 80386 (32 BITS)	INTEL	80287 80387	0.3 WHET/SEC 1.8 WHET/SEC	YES YES	YES, PARTIAL YES, FULL	YES YES	NMOS 40-PIN CMOS 68-PIN PGA	$200 NOW NA 3Q86	IEEE 754 COPROCESSORS FOR 80286 & 80386 µPs. SOME INTERCHANGEABILITY AS 80386 CAN ALSO USE 80287
68000	MOTOROLA	68881	12.5, 16.67 MHz	+, −, x, ÷, $\sqrt{\ }$	TAN, ARCTAN, TANH, LOG E^x, Y^x	YES. 32, 64, 80 BITS	HCMOS +5V 68-PIN	NA NOW	FULL IEEE SPEC FOR FLOATING POINT. WILL SERVE AS COPROCESSOR FOR 68020 AND AS PERIPHERAL TO OTHERS
Z8000 68000 8086/88 GENERAL	ZILOG	Z 8070	10 MHz	+, −, x, ÷, $\sqrt{\ }$	NO (BUT SOFTWARE PACKAGE AVAIL)	YES, 32, 64, 80 BITS	NMOS +5V 68-LCC	NA NOW	FULL IEEE SPECIFICATION. INTERFACES SUITED TO OTHER µPs TO BE ADDED ON FUTURE CHIPS
GENERAL	TRW	TMC 2010	165 nSEC	x, +, −	—	—	CMOS +5V 64-PIN 68-LCC	$114 NOW	16 x 16 = 32 WITH 35-BIT ACCUMULATOR, IN 2-µm CMOS, 0.25W DISS. PIN-COMPATIBLE WITH 1010
GENERAL	INTERSIL	29C510	165 nSEC	x, +, −	—	—	CMOS +5V 64-PIN	$100 2Q86	SIMILAR TO 2010. IN 1.5-µm CMOS
GENERAL	TRW	TMC 2110	100 nSEC	x, +, −	—	—	CMOS +5V 64-PIN 68-LCC	$120 NOW	16 x 16 = 32 WITH 35-BIT ACCUMULATOR, IN 1-µm CMOS, 0.25W DISS. PIN-COMPATIBLE WITH 2010

Continued on pg 133

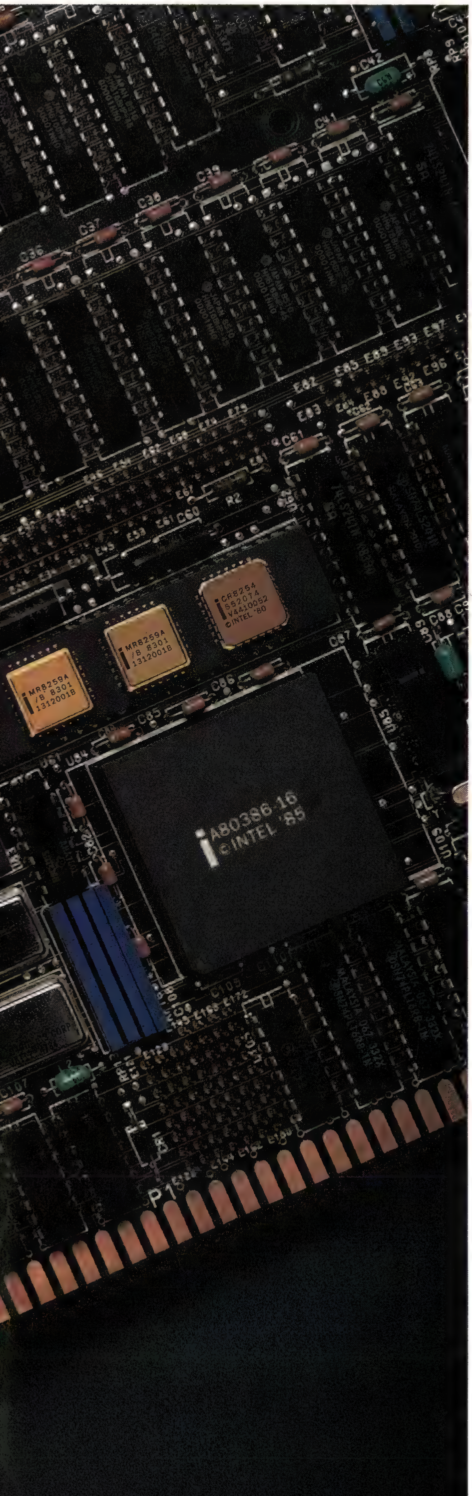
OUR 32-BIT HEAD START PROGRAM.



Just last October, we introduced a 32-bit microprocessor with absolutely blazing speed. Nearly twice the system-level performance of any other.

And now we're shipping our MULTIBUS® I and MULTIBUS II 386 Design Starter Kits.

So you can get your products to market with equally blazing speed.



Whether you're developing high performance systems at the component or board level, these kits will give you a six-month head start.

Both provide everything you need. Including a processor board, a full 32-bit memory board, and a software debug monitor to link to a host.

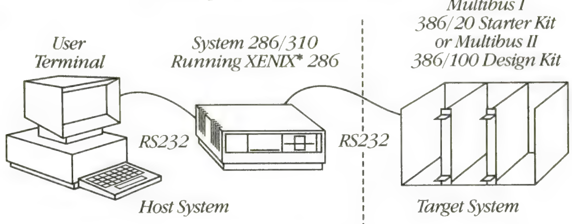
Our MULTIBUS I Starter Kit features the iSBC® 386/20 board. It makes upgrading from existing systems easy. Because it's fully compatible with the most popular bus in the world: MULTIBUS I architecture. And its added speed and power deliver twice the performance of any previous MULTIBUS I processor board. Due, in large part, to the remarkable speed of the 80386. Plus the efficiency of a 32-bit local path to memory. And the turbo-charging of an on-board math coprocessor.

For an even greater leap in system performance, get going with our MULTIBUS II Starter Kit. Its iSBC 386/100 board also utilizes the compatibility features of the 80386.

But coupled with the advanced multiprocessing capability of MULTIBUS II architecture, it gives you all the power of a mainframe. While maintaining access to hundreds of standard off-the-shelf board level products.

Both MULTIBUS I and MULTIBUS II boards have up to 16 MB of local memory. Plus a large on-board cache for zero wait-state memory-to-processor transfer.

Getting Started With the 386



And both boards are supported by all the development tools you need to get to market fast.

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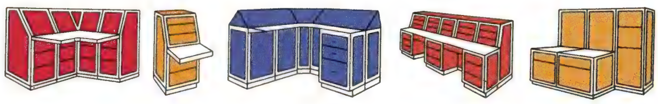

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CIRCLE NO 121

1D NUMBER CRUNCHERS *(continued)*

µP BUS COMPATIBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: MATH	TRIG	FL PT	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	TRW	TDC 1028	10 MHz	x, +	—	—	BIPOLAR +5V 48-PIN	$83 NOW	4 x 4 x 8-TAP FIR FILTER. 2.5W DISS, WORST CASE
GENERAL	WEITEK	WTL 1516 /A/B	50 nSEC 100 nSEC	x	NO	NO	NMOS +5V 64-PIN (LLC, PGA)	$85 $110 NOW	HIGH-SPEED, LOW-POWER 16-BIT MULTIPLIER WITH FULLY MULTIPLEXED OUTPUT
GENERAL	INTERSIL	29C516	100 nSEC	x	—	—	CMOS +5V 64-PIN	$75 2Q86	SIMILAR TO 2016. IN 1.5-µm CMOS
GENERAL	WEITEK	WTL 1064 1065 1264 1265	4M FLOPS 240 nSEC FOR 32 x 32 8M FLOPS 120 nSEC FOR +, − 2x SPEED OF 1064/65	x +, −	NO	YES	NMOS +5V 144-PIN GRID-ARRAY NMOS +5V 144-PIN GRID-ARRAY	$795 FOR 1064/65 SET NOW $795 FOR 1264/65 CHIP SET NOW	SINGLE OR DOUBLE PRECISION FLOATING PT MULTIPLIER (1064) & ALU (1065). IEEE 754 PIPELINED. FOR VECTOR PROCESSING
GENERAL 80386	WEITEK	1164 1165 1163	180-nSEC SINGLE PREC, 300-nSEC DOUBLE PREC (4M WHET/SEC)	x +, −	NO	YES	NMOS +5V 64-PIN 68-LCC	$580 PER 64/65 SET NOW 1Q86	SINGLE- OR DOUBLE-PRECISION FLOATING PT MULTIPLIER (1164) & ALU (1165). LOW LATENCY SCALAR OPERATION. 1163 INTERFACES 1164/65 TO 80386

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

1E INTERRUPT CONTROLLERS

EXPAND, PRIORITIZE, AND PROVIDE INTERRUPT VECTOR ADDRESSING FOR µPs.

µP BUS COMPATIBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: PRIORITY LEVELS	EXPANDABLE	PROGRAMMABLE	INTERRUPT MASKING	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
8080/85 8086/88 NSC800	HARRIS OKI VTI INTERSIL	82C59A	8-MHz µP CLOCK	8	YES, TO 64 LEVELS	YES	YES	CMOS +5V 28-PIN PLCC	$3.70 NOW	OPERATES IN EITHER 8080/85 OR 8086/88 CALL MODE
68000	MOTOROLA	68153 BIN	16 MHz	7	—	YES	—	BIPOLAR 28-PIN	$50 NOW	ROUTES INTERRUPTS FROM 4 INDEPENDENT SOURCES TO ANY OF 7 68000 INTERRUPT LEVELS
VME OR VERSA BUS	SIGNETICS	SCB 68154 (IGOR)	11 MHz	7	—	—	YES	BIPOLAR 40-PIN	$15 NOW	INTERRUPT GENERATOR PROVIDING FOR VME OR VERSA BUS, GENERATES 7 BUS INTERRUPT REQUESTS
VME BUS	SIGNETICS	SCB 68155 (IVHAN)	10 MHz	7	—	—	YES	BIPOLAR 40-PIN	$15 NOW	INTERRUPT HANDLER. ACCEPTS INTERRUPTS FROM 14 SOURCES. LOCAL MASTER IACK CYCLE WITH VECTOR FROM 68154
GENERAL	AMD	9519A	—	—	YES	YES	YES 8 INPUTS	NMOS 28-PIN	$17.50 NOW	UNIVERSAL INTERRUPT CONTROLLER
32000	NATIONAL TI	32202 ICU	6, 8, 10 MHz	16	YES, CASCADABLE TO 240	YES	YES	NMOS +5V 40-PIN	$33 NOW	ALSO TWO 16-BIT TIMERS, 8 PARALLEL I/O LINES. FIXED OR ROTATING PRIORITIES
NSC800 8080/85 Z80 8086/88	NATIONAL	NSC859	4 MHz	8	—	YES	YES	CMOS +5V 28-PIN	NA 1H86	COMPATIBLE WITH ALL NSC800/Z80 MODE 0, 1, 2 INTERRUPTS
Z8000	ZILOG AMD SGS	Z 8036 8536	4, 6 MHz	16	YES, CASCADABLE	YES	YES	NMOS +5V 40-PIN	$7.07 NOW	ALSO THREE 16-BIT TIMERS & TWO 8-BIT AND ONE 4-BIT PORTS. 8036 IS FOR MUXED BUS

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

1F DMA CONTROLLERS

TAKE OVER µP BUSES AND ACT AS SPECIAL-PURPOSE µPs TO CONTROL ADDRESS BUS AND MOVE BLOCKS OF DATA. FUNCTION AS COPROCESSOR.

µP BUS COMPATIBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: CHANNELS	MODES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
6800 6809	MOTOROLA	6844	2 MHz	4	3	NMOS 40-PIN	$12.65 NOW	2M-BYTES/SEC TRANSFER RATE

1F DMA CONTROLLERS *(continued)*

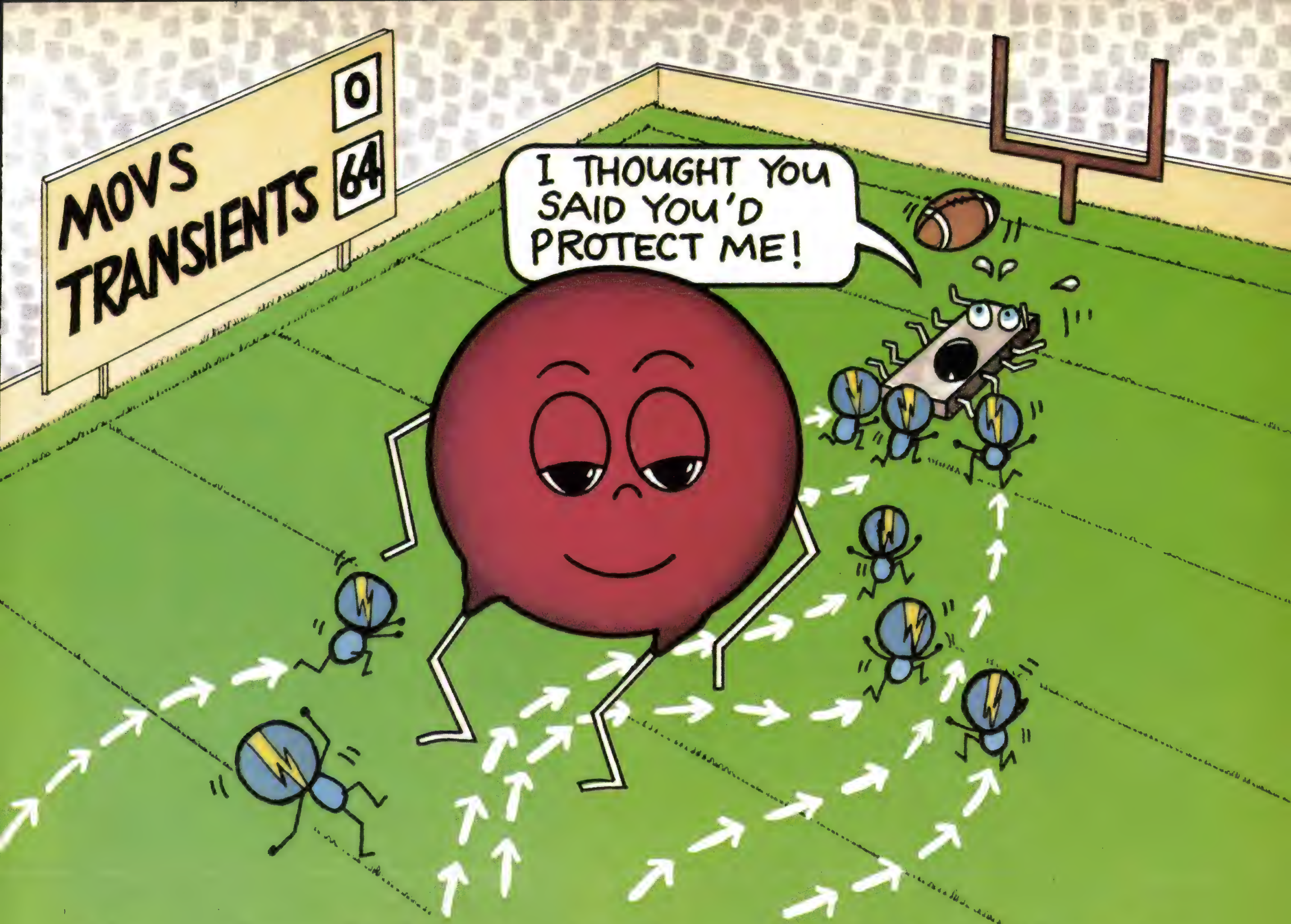
μP BUS COMPATIBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: CHANNELS	KEY SPECIFICATIONS: MODES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
68000	SIGNETICS	SCB 68430 DMAI	10, 12.5 MHz	1	READ, WRITE BURST, CYCLE STEAL	ISL +5V BIPOLAR 48-PIN	$14 NOW	5M-BYTES/SEC MAX DATA TRANSFER. SUPPORTS 32-BIT TRANSFER ON VME BUS. 2 YRS LATE
68000	HITACHI MOTOROLA	68440 DDMA	8, 10, 12 MHz	2	BURST, CYCLE STEAL, LRAR	HMOS +5V 64-PIN 68-PGA	$33.55 NOW	6.25M BYTES/SEC AT 12.5 MHz. PROGRAMMABLE BUS UTILIZATION IN LRAR MODE
68000	MOTOROLA	68442	8, 10 MHz	2	BURST, CYCLE STEAL, LRAR	HMOS +5V 68-PGA	$56 NOW	6.25M BYTES/SEC AT 12.5 MHz. PROGRAMMABLE BUS UTILIZATION IN LRAR MODE. FULL 32-BIT LINEAR ADDRESS
68000	HITACHI MOTOROLA	68450 DMAC	8, 10 MHz	4	BURST, CYCLE STEAL, LRAR, ARRAY, AND LINKED ARRAY CHAINING DATA TRANSFERS	HMOS +5V 64-PIN 68-PGA	$46.67 NOW	5M BYTES/SEC MAX AT 10 MHz ARRAY AND LINKED-LIST CHAINING
Z80	TOSHIBA ZILOG	Z80C DMA, Z84C10	DC-4 MHz 2M BYTES/SEC	1	BYTE-AT-TIME, BURST, CONTINUOUS TRANSFER, SEARCH OR TRANSFER/SEARCH	CMOS +5V 40-PIN 44-PIN FLAT PACK	$15.95 $9.80 1Q86	CMOS VERSION OF NMOS Z8410. SUPPORTS DAISY-CHAIN INTERRUPTS & DMA REQUESTS
8086/88	AMD	9517A	5 MHz	4	SINGLE, BLOCK, DEMAND, CASCADE	NMOS +5V 40-PIN	$7.25 NOW	ONE OF THE EARLIER DMA DEVICES
8086/88 80186/188 80286	INTEL	82258	8M BYTES/SEC IN 80286 SYSTEMS	4	COMMAND & DATA CHAINING, 32 SUB CHANNELS. TRANSLATE & ASSEMBLY/DISASSEMBLY OPERATIONS DONE ON THE FLY	NMOS 68-PIN LCC	$150 NOW FOR 6 MHz 2H86 FOR 8 MHz	SAID TO BE DESIRABLE FOR HARD-DISK SYSTEMS SUCH AS IBM PC/AT
V SERIES 8 OR 16 BITS	NEC	71071	2 MHz 5.33M BYTES/SEC MAX	4	RELEASE & HOLD MODES FOR SINGLE, DEMAND, AND BLOCK TRANSFER	CMOS +5V 48-PIN	$11.40 NOW	HAS 16-BIT DATA BUS AND 24-BIT ADDRESS BUS. CAN BE USED TO UPGRADE DESIGNS WITH MINIMAL SOFTWARE CHANGES

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

1G MEMORY (INCLUDING VIRTUAL MEMORY AND CACHE) AND BUS CONTROLLERS (INCLUDING BACKPLANE)

THIS SECTION HAS BECOME A CATCHALL. ORIGINALLY JUST INCLUDED REFRESH EXCITATION FOR DYNAMIC MEMORIES, BUT NOW INCLUDES BUS SUPPORT DEVICES FOR COMPLICATED BUSES SUCH AS VME AND MULTIBUS.

μP BUS COMPATIBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: CHANNELS, ETC	KEY SPECIFICATIONS: MODES, ETC	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	NATIONAL	DP 8419-70	10–20 MHz NO WAIT STATES (70 nSEC)	16k-, 64k-, 256k-BIT DRAMs	70 nSEC RASIN TO CAS LOW UNDER 500-pF LOADS. AUTOACCESS AUTOREFRESH	BIPOLAR ALS TTL +5V 48-PIN, 68-PCC	$32 NOW	GENERAL 256k DRAM CONTROLLER, ALL MAJOR μPs. COMPATIBLE WITH 8408/9. ONBOARD BUFFER DRIVERS, DELAY LINE, ECC
GENERAL	NATIONAL	DP 8409A DP 8408A	8-MHz CPUs NO WAIT STATES (130 nSEC)	16k, 64k, 256k BITS 16k, 64k BITS	130 nSEC RASIN TO CAS LOW UNDER 500-pF LOADS. AUTOACCESS AUTOREFRESH	BIPOLAR LSTTL +5V 48-PIN 68-PCC	$25 NOW $13.90 NOW	A GENERAL 256k DRAM CONTROLLER, ALL MAJOR μPs. ONBOARD BUFFER DRIVERS & DELAY LINE
GENERAL	NATIONAL	DP 84300	12.5-MHz CPUs	—	USER SELECTS NUMBER OF INPUT CLOCK CYCLES PER REFRESH PERIOD	BIPOLAR SCHOTTKY +5V 24-PIN	$5.75 NOW	PROGRAMMABLE REFRESH TIMER. SUPPORT FOR DP 8408A–8429 DRAM CONTROLLERS
GENERAL	NATIONAL	DP 8400-4 DP 8400-2	55 nSEC DATA TO CORRECT OUT	—	16-BIT ERROR CHECK & CORRECT, EXPANDS TO 64 BITS. CAN DETECT 3 ERRORS, CORRECT 2	BIPOLAR SCHOTTKY +5V 48-PIN 68-PCC	$40 NOW $45 NOW	-2 IS UPGRADE OF -4, CONSUMING 25% LESS POWER. CASCADABLE TO OVER 64 BITS. USES MODIFIED HAMMING CODE
GENERAL	NATIONAL	DP 8402A SN 74ALS 632A	55 nSEC DATA IN TO CORRECT OUT	—	32-BIT PARALLEL ERROR DETECTION/CORRECTION. GENERATES 7 CHECK BITS	BIPOLAR ALS +5V 52-PIN 68-PCC	$100 NOW	CORRECTS 1-BIT ERRORS & FLAGS 2-BIT ERRORS. USES MODIFIED HAMMING CODE
32008 32016 32032	NATIONAL	DP 84412	10 MHz 32000 NO WAIT STATES	—	INTERFACES BETWEEN CPU & 8408A TO -29 DRAM CONTROLLER/DRIVERS	BIPOLAR SCHOTTKY +5V 20-PIN	$3.75 NOW	A FAST HAL 16R4; STD PAL 16R4A CAN BE USED. MFG PROVIDES LOGIC EQUATIONS
68000 68008 68010	NATIONAL	DP 84322 DP 84422	10 MHz 12.5 MHz 68000+ NO WAIT STATES	—	INTERFACES BETWEEN CPU & 8408A TO -29 DRAM CONTROLLER/DRIVERS	BIPOLAR SCHOTTKY +5V 20-PIN	$3.75 NOW	A FAST HAL 16R4; STD PAL 16R4A CAN BE USED. MFG PROVIDES LOGIC EQUATIONS
8086/88 186/188	NATIONAL	DP 84432	10 MHz 8086+ NO WAIT STATES	—	INTERFACES BETWEEN CPU & 8408/09/19 DRAM CONTROLLER/DRIVERS	BIPOLAR SCHOTTKY +5V 20-PIN	$3.75 NOW	A FAST HAL 16R4; STD PAL 16R4A CAN BE USED. MFG PROVIDES LOGIC EQUATIONS



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The true test of any transient voltage suppressor is the **Clamping Voltage**—the voltage appearing across the device when subjected to a high-energy transient pulse. In many instances, there is no direct relationship to the Joule rating of a suppressor and the Clamping Voltage. Experiments show that a 5 volt NMOS 64K RAM will fail destructively with momentary excursions over the 13.5 volt V_{cc} limit[1]. Even low-energy ESD pulses can contain currents in excess of 50 amps. Low-voltage metal oxide varistors, which will allow transients in excess of 25 volts to pass into your circuits, **will not** protect your ICs from upset and/or destruction.

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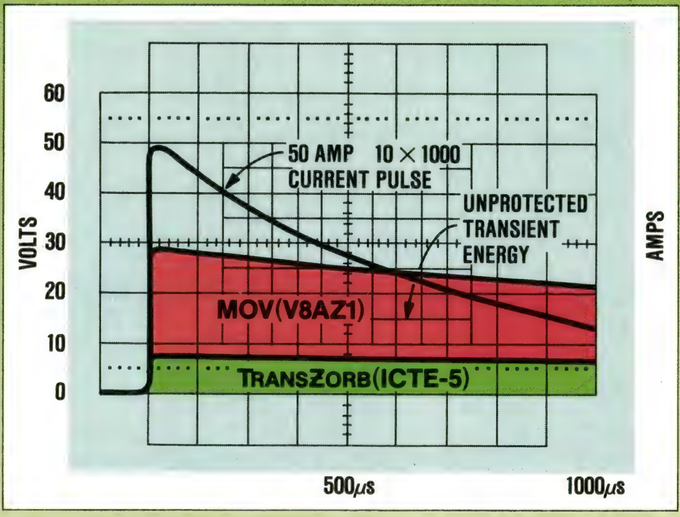

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[1] Zaremba/Mansmann, Motorola, Inc., Powerconversion & Intelligent Motion, October, 1985.

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Device	Access Times	Max Power (mW) act	stby	Process
IMS1400 16K x 1	35,45,55	660	110	NMOS
IMS1420 4K x 4	45,55	605	165	NMOS
IMS1423 4K x 4	25,35,45	660	33 CMOS	CMOS
IMS1600 64K x 1	45,55,70	440	77 CMOS	CMOS
IMS1620 16K x 4	45,55,70	440	77 CMOS	CMOS

CIRCLE NO 123

inmos

1G MEMORY (INCLUDING VIRTUAL MEMORY AND CACHE) AND BUS CONTROLLERS (INCLUDING BACKPLANE) *(continued)*

µP BUS COMPATIBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: CHANNELS, ETC	KEY SPECIFICATIONS: MODES, ETC	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL 16-BIT	NATIONAL	DP 8417 DP 8418	10–20 MHz (70 nSEC RASIN TO CAS LOW AT 500-pF LOADS)	16k-, 64k-, 256k-BIT DRAMs	FOUR MODES. AUTOMATIC OR EXTERNALLY CONTROLLED ACCESS & REFRESH. NIBBLE/PAGE MODE SUPPORTED	BIPOLAR ALS +5V 52-PIN 48-PIN 68-PIN	$32 NOW $32 NOW	256k DRAM CONTROLLER/DRIVER TAILORED FOR 16-BIT WORD PLUS ERROR-CORRECTION BITS. 3-STATE OUTPUTS FOR EXPANSION
GENERAL 32-BIT 16-BIT	NATIONAL	DP 8428 DP 8429	20 MHz (70 nSEC RASIN TO CAS LOW AT 500-pF LOADS)	ALL 1M-BIT DRAMs	FOUR MODES. AUTOMATIC OR EXTERNALLY CONTROLLED ACCESS & REFRESH. NIBBLE/PAGE MODE SUPPORTED	BIPOLAR ALS +5V 52-PIN 68-PIN PCC	$37.50 NOW $37.50 1Q86	1M-BIT DRAM CONTROLLER/DRIVER FOR 32- & 16-BIT WORDS, RESPECTIVELY, PLUS ERROR-CORRECTION CHECK BITS
68020 80286	NATIONAL	DP 84522 DP 84532	10–20 MHz	—	PROVIDES COMPLETE INTERFACE BETWEEN MOTOROLA 68020 & INTEL 80286 µPs RESPECTIVELY & NATIONAL SERIES DRAM CONTROLLERS	BIPOLAR ALS 20-PIN	$3.75 1Q86	A FAST HAL 16R4A; STD PAL 16R4 MAY BE USED & TAILORED TO SYSTEM REQUIREMENTS. DATA SHEET HAS BOOLEAN EQUATIONS
GENERAL ("OPEN") 8086, 68000, ETC	TOSHIBA VTI INTEL	BUS INTERFACE CHIP	40M BYTES/SEC (MULTIBUS II)	—	ISO LEVELS 1, 2, 3, 4. INCLUDES BUS ARBITRATION, BUS PARITY GENERATION/CHECKING, & FULL MESSAGE PASSING (LEVEL 4)	CMOS NA (OVER 100 PINS)	NA 2Q86	INTERFACES BETWEEN CPU CARD AND MULTIBUS-II BACKPLANE. SAID TO BE 3 TO 5 TIMES FASTER FOR MULTIPROCESSING BECAUSE PERFORMS MESSAGE PASSING IN HARDWARE
GENERAL	INTEL	82C08	8 MHz	64k- & 256k-BIT DRAMs	AUTOMATIC RAM WARM-UP. 5 PROGRAMMABLE REFRESH MODES. POWER-DOWN REFRESH.	CMOS +5V 48-PIN	NA NOW	INTERFACES DYNAMIC RAMs UP TO 1M BYTE ADDRESS
80286	AMD	82C288	6–12.5 MHz	—	PROVIDES ADDRESS LATCH CONTROL, DATA TRANSCEIVER CONTROL & STANDARD LEVEL COMMAND OUTPUTS.	CMOS 20-PIN	$26.80 NOW	BUS CONTROLLER FOR 80286 µP. ALLOWS FLEXIBLE TIMING OPTIONS & HAS SEPARATE COMMAND OUTPUTS FOR MEMORY & I/O
68000	MOTOROLA	68451 MMU	8, 10 MHz	—	TRANSLATION, RELOCATION, PROTECTION	HCMOS 64-PIN 68-PIN PGA	$46.33 NOW	IDEAL MMU FOR NONDEMAND-PAGED 68000 & 68010 µPs
68000	MOTOROLA	68452 BAM	52 nSEC ARBITRATION TIME	—	LOCAL CENTRAL & GLOBAL BUS ARBITER, CASCADABLE	BIPOLAR 28-PIN	$25 NOW	ARBITRATES ACCESS OF 68000 SYSTEM BUS BETWEEN µP TO 8 LOCAL MASTERS
68000	MOTOROLA	68461 MMC	16.67 MHz	—	TRANSLATION, RELOCATION, PROTECTION	BIPOLAR 149-PIN	$300 NOW	GATE-ARRAY IMPLEMENTATION OF 68851 FUNCTIONAL SUBSET
68000	MOTOROLA	68851 PMMU	12.5, 16.67 MHz	—	SINGLE CYCLE TRANSLATION, PROGRAMMABLE PAGE SIZES	HCMOS 124-PIN PGA	$325 NOW	32-BIT DEMAND VIRTUAL PAGED MEMORY-MANAGEMENT UNIT FOR 68020- OR 68010-BASED SYSTEMS
VME BUS	SIGNETICS	SCB68171	2.9M BPS	MULTIPLE	CONNECTS ONE OR MORE VMS BUS CONTROLLERS TO VMS BUS. PROVIDES BUS DRIVING & RECEIVING	BIPOLAR 16-PIN	$15 2H86	INTERFACE DEVICE FOR SCC68173
VME BUS	SIGNETICS	SCB68172 BUSCON	25 MHz	LOCAL & SYSTEM BUSES & DUAL-PORTED OPERATION	NORMAL BUS CYCLE, BLOCK XFR, RELEASE ON REQUEST, RELEASE WHEN DONE	BIPOLAR +5V 28-PIN	$27 NOW	VME BUS CONTROLLER, MASTER/SLAVE, DEADLOCK ARBITRATION, SINGLE RETRY ON ERROR, BUFFER CONTROL
VMS BUS	SIGNETICS	SCC68173	2.9M BPS	SERIAL & LOCAL PROCESSOR BUS	4 PROGRAMMABLE. DOES NOT REQUIRE ONBOARD INTELLIGENCE	CMOS +5V 28-PIN	$15 2H86	SERIAL (VMS) BUS CONTROLLER. COMPANION CHIP TO 68171
VME	SIGNETICS	SCB68175 (8 x 821)	25 MHz	—	ASYNC BUS CONTROL FOR VME BUS & VERSABUS MASTERS. SUPPORTS RELEASE-ON-REQUEST & RELEASE-WHEN-DONE. BUS ERROR/RETRY SEQUENCING	BIPOLAR 24-PIN	$15 NOW	BUS MASTER
68000	SIGNETICS	SCC68005 SCC68006	10, 12.5 MHz	24-BIT ADDRESS 32-BIT ADDRESS	BASIC MEMORY ACCESS CONTROLLERS FOR 68010 & 68020 µPs	CMOS +5V 84-PIN 120-PIN	$50 $60 3Q86 3Q86	SAME AS 68910 AND 68920, RESPECTIVELY, BUT ERROR HANDLING MUST BE DONE BY USER (VIA SOFTWARE)
68000	SIGNETICS	SCC68910 SCC68920	12.5 MHz 16.7 MHz	24-BIT ADDRESS 32-BIT ADDRESS	SUPPORTS CACHE MEMORY, LOCAL MEMORY & VARIABLE-LENGTH CONTIGUOUS SEGMENTS & PAGED ONLY	CMOS +5V 84-PIN 120-PIN	NA 4Q86	MEMORY ACCESS CONTROLLER FOR 68010 AND 68020 µPs RESPECTIVELY. (DEMAND-DRIVEN MMU.) ERROR CORRECTION BY HARDWARE. PAGED ONLY
GENERAL	TI	4500A	150, 200 nSEC	CONTROLS 64k-BIT DRAMs	8 REFRESH MODES, FREQUENCIES	NMOS +5V 40-PIN	$15 NOW	DRAM CONTROL WITH ON-CHIP TIMING & ARBITRATION
GENERAL	TI	4502	125 nSEC	CONTROLS 256k-BIT DRAMs	8 REFRESH MODES, FREQUENCIES	CMOS +5V 48-PIN	$18 NOW	DRAM CONTROL WITH ON-CHIP TIMING & ARBITRATION
GENERAL	TI	2150	35, 45, 55 nSEC	8-BIT, EXPANDABLE	—	NMOS +5V 24-PIN	$25 NOW	CACHE ADDRESS COMPARATOR
GENERAL 8, EXP TO 16, 32	TI	9650 MPIF	3.7M BYTES/SEC	4 (DATA A, DATA B, CONTROL A, CONTROL B)	2 (STAND-ALONE, MASTER, SLAVE)	NMOS +5V 40-PIN	$6.90 NOW	ALLOWS TWO µPs TO INTERFACE VIA ITS COMMON 256 BYTES RAM

1G MEMORY (INCLUDING VIRTUAL MEMORY AND CACHE) AND BUS CONTROLLERS (INCLUDING BACKPLANE) *(continued)*

μP BUS COMPAT-IBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: CHANNELS, ETC	KEY SPECIFICATIONS: MODES, ETC	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	TI	ALS632	58-nSEC CORREC-TION TIME	—	32-BIT EDAC WITH DIAG-NOSTICS & BYTE-WRITE	BIPOLAR ALS +5V 52-PIN	$92 NOW	DETECTS & CORRECTS SINGLE-BIT ERRORS. DETECTS & FLAGS DUAL-BIT ERRORS
GENERAL	TI	ALS616	65-nSEC CORREC-TION TIME	—	16-BIT EDAC WITH DIAG-NOSTICS & BYTE-WRITE	BIPOLAR ALS +5V 40-PIN	$46 NOW	DETECTS & CORRECTS SINGLE-BIT ERRORS. DETECTS & FLAGS DUAL-BIT ERRORS
GENERAL (FLEXIBLE WORD WIDTH)	MMI	674219	24 MHz, 6–12 MHz DATA RATE. (NO FALL-THROUGH TIME)	—	PROVIDES ADDRESS & CON-TROL SIGNALS TO SRAMs & INTERFACES WITH μP SYS-TEM THROUGH R/W PORTS & STATUS FLAGS	BIPOLAR 40-PIN	$28.35 NOW	FOR TURNING AN ARRAY OF SRAMs INTO A FIFO BUFFER WITH 512 TO 65k WORDS OF INDEFINITE WIDTH (NEEDS 2 AUXILIARY REGISTERS)
32010	PACIFIC MICRO-CIRCUITS	32HC01 32HC02 32HC03	5–6.25 MHz	—	INTERFACES 32010 TO RAM, ROM, AND CODEC, FOR REAL-TIME DSP	CMOS +5V 40-PIN	$10 NOW NOW 2Q86	CONSOLIDATES GLUE PARTS FOR TYPICAL 302010 DSP μP SYSTEM. FOR INTERFACING TO MEMORY & I/O

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

1H SYSTEM FIRMWARE

ROMABLE SOFTWARE OF INTEREST TO OEM DESIGNERS. INCLUDES OPERATING-SYSTEM KERNELS, POPULAR INTERPRETED-TYPE HIGH-LEVEL LANGUAGES, MATH SUBROUTINES, ETC. TYPICALLY AVAILABLE ON ROMs OR ON DISKS.

μP BUS COMPAT-IBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: ROM FIRM-WARE	KEY SPECIFICATIONS: RAM REQ (BYTES)	KEY SPECIFICATIONS: OTHER FEATURES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
Z80 8080/85 8086/88 68090 68000 32000 LSI-11 WE32100	JMI	C EXEC-UTIVE	—	5k–7k x 8	—	PROVIDES INTERRUPT-DRIVEN DEVICE DRIVERS & PRIORITIZED SCHEDULING, ETC. MOSTLY IN C LAN-GUAGE. OP-TIONAL FILE SYSTEM	(BY CUSTOMER)	$70 (LIC) NOW	ROMABLE SOFTWARE THAT PER-MITS MULTIPLE C AND PASCAL PROGRAMS TO RUN FROM MAIN MEMORY WITHOUT DISK
8048 8051 7809 7810 Z8 ZS8	MICRO COMPUTER CONTROL	MICRO/OS	VARIES WITH TARGET μP	368 x 8	8 BYTES/ TASK + REGISTER + TIMER	TIME MAN-AGEMENT 1-TASK SCHEDULING 2-TASK SWITCHING 3-INTERRUPT MANAGEMENT (16 TASKS)	(BY CUSTOMER)	$45 NOW	REAL-TIME MULTITASKING EXEC-UTIVE FOR SMALL 1-CHIP μCs. PRE-EMPTIVE PRIORITIZED TASK SCHEDULING
6800 68000 8080/85 Z80 8086/186	INDUSTRIAL PROGRAM-MING INC	MTOS MTOS-UX	VARIES WITH TARGET μP	3k–16k x 8	½k–1k	MTOS IS STANDARD VERSION. NEWER MTOS-UX HAS LINKS TO UNIX	(BY CUSTOMER)	$4k–$12k ($350–$400 LIC COST PER USER)	SOPHISTICATED REAL-TIME MULTI-TASKING, MULTI-μP OPERATING SYSTEM. IS BEING USED WITH 64 μPs ON BUS
680XX 8086/88 80186/88 80286 80386 Z80 Z8002 32000	H&R	VRTX	(LIST, TIMES/ TASK AVAIL)	4k x 8	1k	COMPLETE REAL-TIME MULTITASKING, INCLUDING MUTUAL EXCLUSION, SIGNALING & MESSAGE QUEUING	TWO 24-PIN EPROMs	$70 NOW	VRTX (VERSATILE REAL-TIME EXEC-UTIVE) IS CENTRAL COMPONENT: OTHERS FOR I/O, FILE MANAGE-MENT & REAL-TIME DEBUGGING. PRICING IS BY PIECE & DOESN'T INCLUDE "UP-FRONT" COSTS
680XX 8086/88 80186/88 Z80 Z8002	H&R	IOX	(LIST, TIMES/ TASK AVAIL)	24k x 8	1k MIN	SUPPORTS DISK, BLOCK, CHAR, & SPE-CIAL DEVICES IN REAL-TIME MULTITASKING	TWO 24-PIN EPROMs	$70 NOW	I/O DRIVERS AVAIL FOR IBM PC/XT/AT, INTEL 208/215/218, XEBEC S1410 DISK CONTROL & MOTOROLA VME10
680XX 8086/88 80186/88 Z80 Z8002	H&R	FMX/DOS	(LIST, TIMES/ TASK AVAIL)	24k x 8	1k MIN	REAL-TIME FILE MANAGER PRODUCING HIERARCHICAL FILES COM-PATIBLE WITH PC-DOS 2.0	TWO 24-PIN EPROMs	$35 NOW	I/O DRIVERS AVAIL FOR IBM PC/XT/AT, INTEL 208/215/218, XEBEC S1410 DISK CONTROL & MOTOROLA VME10

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

Continued on pg 143

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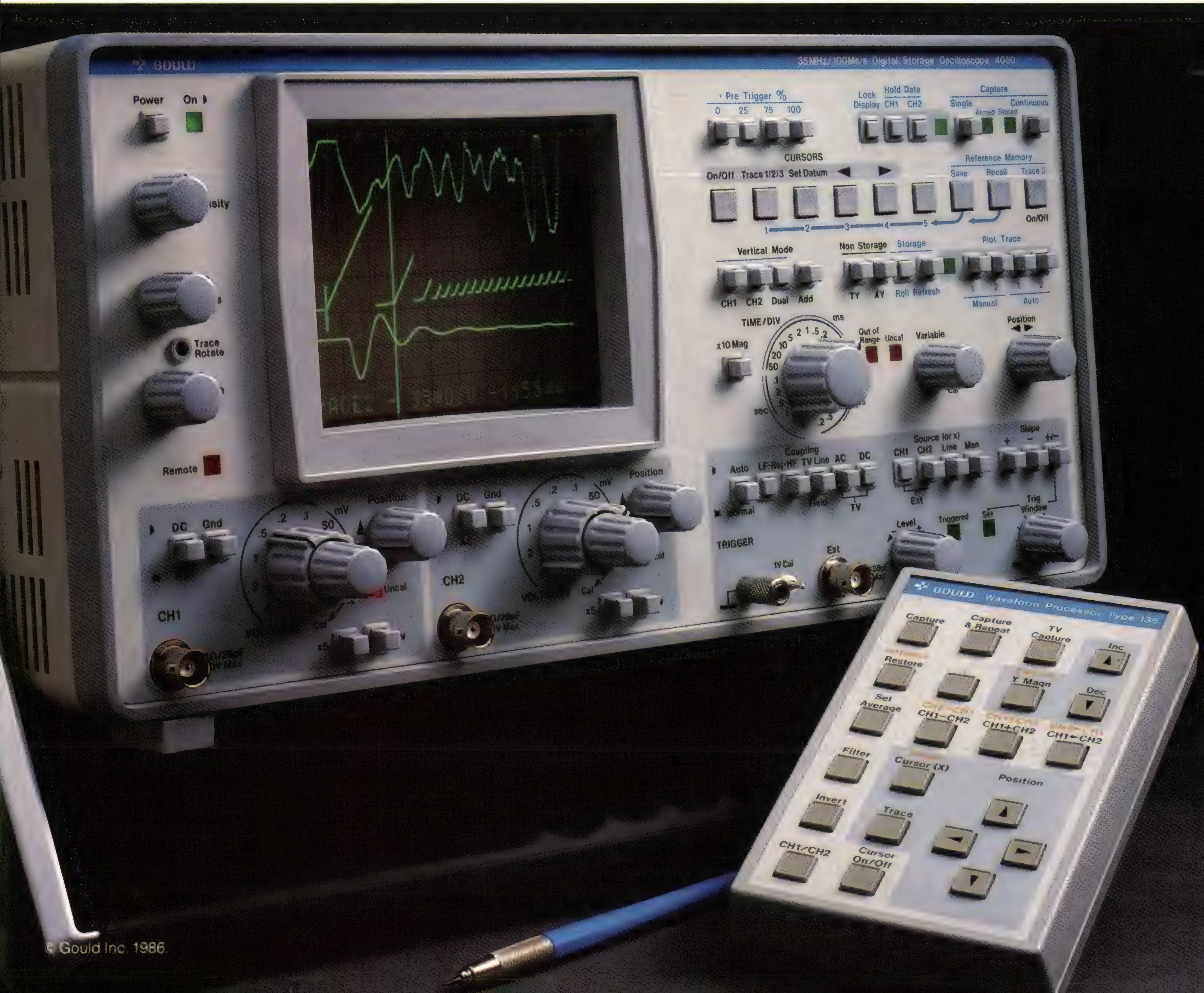
CIRCLE NO 124



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Conductor thickness typical, (Inches x 10^{-3})	0.1-3.0	0.8	0.05
Circuit resolution (Conductors/inch/layer)	200	90	150
Typical circuit layers	2	1-3	1
Conductor adhesion (Lb/in^2)	$>$ 2000	1000	2000
Adhesion after heat aging (150 hr @ 175°C)	1800	850	1800
Wire bond strength (Grams)	13-15	8-11	13-15
Bond strength after aging (24 hr @ 160°C)	12-14	7-9	12-14

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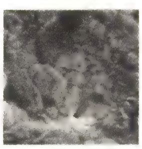

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CIRCLE NO 191

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CIRCLE NO 126

1I SYSTEM GLUE

THESE ARE THE BUS BUFFERS, DRIVERS, TRANSCEIVERS, ADDRESS DECODERS, CONTROL LOGIC GATES, ETC THAT UNITE THE MAIN LSI PARTS OF A μP SYSTEM. LISTED IS A SMALL, RANDOM SAMPLING OF THE MANY THOUSANDS OF DEVICE TYPES AVAILABLE. FOR A MORE COMPLETE PICTURE, CONSULT STANDARD CATALOGS FOR BIPOLAR TTL, CMOS TTL, ECL LOGIC, ETC. KEEP IN MIND THAT MANY OF THESE PARTS ARE NOW ALSO IN MOST SEMICUSTOM-CELL LIBRARIES.

μP BUS COMPAT-IBILITY	SUPPLIER	PART NO	KEY SPECIFICATIONS		TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
			FUNCTIONS	SPEED			
GENERAL	SIGNETICS	FAST 74F455 655A 456 656A 657	OCTAL BUFFER/TRANS-CEIVERS PLUS 9TH PARITY BIT	3.5-nSEC PROPAGATION DELAY (8 nSEC FOR F675)	BIPOLAR 24-PIN	$3.90 NOW	VERSIONS OF POPULAR 240 OCTAL TRANSCEIVERS WITH ADDED PAR-ITY BIT AND PARITY GENERATOR/CHECKER LOGIC
GENERAL	ZILOG	8060 8038	OCTAL BUFFER, 128 DEEP	NA	NMOS 28-PIN 40-PIN	NA 1986	FIFO FOR CONNECTING ASYNCHRONOUS DEVICES
6500 6800	WDC	65C90	OCTAL INPUT CAN BE COMPARED TO INTERNAL DATA REGISTER	CMOS +5V 24-PIN	CMOS +5V 24-PIN	NA 1986	8-BIT CASCADABLE COMPARA-TOR, EACH BIT MASKABLE TO DON'T CARE
GENERAL	MOTOROLA	74HC9014 9015 9114 9115	9-WIDE SCHMITT TRIG-GER, INVERTING & NONINVERTING, & WITH OPEN-DRAIN OPTION	25–30 MHz	CMOS 2–6V	NA 2Q86	FOR USE WHEN AN EXTRA BIT IS NEEDED FOR PARITY (OR FOR CONTROL OR HANDSHAKING)
GENERAL	MOTOROLA	74HC9034 HCT9034 HC9035 HCT9035 HC9134 HC9135	9-WIDE BUFFER, INVERT-ING OR NONINVERTING, WITH OPEN-DRAIN OPTION	25–30 MHz	CMOS	NA 1Q86 2Q86	HAS EXTRA (9TH) BIT FOR PARITY OR CONTROL
80C86/88 GENERAL	HARRIS	82C82 82C83	OCTAL LATCH	8 MHz	CMOS +5V 20-PIN	$4.69 NOW	82C83 HAS INVERTING OUTPUTS
80C86/88 GENERAL	HARRIS	82C86 82C87	OCTAL BUS TRANSCEIVER	8 MHz	CMOS +5V 20-PIN	$6.65 NOW	82C87 HAS INVERTING OUTPUTS
GENERAL	NATIONAL	DP 83BC03 83BC04	OCTAL BUS TRANSCEIVER	10 MHz	BIPOLAR/CMOS 20-PIN	$2.25 NOW	PIN COMPATIBLE WITH 82C86, 82C87
GENERAL	TRW	TDC 1011	VARIABLE-LENGTH SHIFT REGISTER	18 MHz	BIPOLAR 20-PIN	$20 NOW	

NOTE:
SOME OF THE MANY SOURCES FOR GLUE LOGIC ARE: RCA, SIGNETICS, MOTOROLA, NATIONAL SEMICONDUCTOR, MMI, TI, FAIRCHILD, MITEL, GTE, SGS, TOSHIBA, SSS, SUPERTEX, ZYTREX, IDT, FUJITSU. ALSO, MANY OF THE SEMICUSTOM SUPPLIERS OFFER THE STANDARD TTL FUNCTIONS AS PART OF THEIR CELL LIBRARIES, OR CAN EASILY CREATE THE FUNCTIONS FROM EASILY OBTAINABLE LOGIC DIAGRAMS.

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

TABLE 2—COMBINATION CHIPS

THESE DEVICES COMBINE SEVERAL SUPPORT AND μC-SYSTEM FUNCTIONS. WERE POPULAR BECAUSE THEY PERMITTED THE CONFIGURATION OF ECONOMICAL 2-CHIP SYSTEMS. NOW TREND IS TO USE VLSI ADVANCES TO COMBINE FUNCTIONS WITH CPU.

μP BUS COMPAT-IBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS				TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
				ROM	RAM	PORT BITS	TIMERS			
6500	ROCKWELL	6531	2 MHz	2k x 8	128 x 8	8, 8, +4 HAND-SHAKE	1 x 16	NMOS +5V 40-PIN	$16.90 NOW	ROM HAS BEEN USED TO CARRY MONITOR OR SIMPLE OPERATING SYSTEM
6500 6800	GTE WDC	65C32	1–4 MHz	—	128 x 8	8, 8, +4 HAND-SHAKE	1 x (16)	CMOS +5V 40-PIN	$4.75 NOW	DIRECT REPLACEMENT FOR NMOS 6532
8051 8085	OKI INTERSIL	81C55	NA	—	256 x 8	8, 8, 6	1 (14-BIT)	CMOS +5V 40-PIN	$5.50 NOW	CMOS VERSION OF INTEL NMOS 8155, INTENDED FOR 2-CHIP 8085 SYSTEMS. STATIC OPERATION. SQUARE-WAVE TIMER
8051 8085	OKI INTERSIL	83C55	NA	2k x 8	—	8, 8	—	CMOS +5V 40-PIN	$6.25 NOW	CMOS VERSION OF INTEL NMOS 8355. CUSTOM ONLY IN VOLUME BECAUSE OF MASKED ROM
8085 8086/88	INTEL SIEMENS	8256 MUART	2–8 MHz μP CLOCK	—	—	8, 8 5=UART WITH BAUD RATE GEN	5 8-BIT CASCAD-ABLE TO 2 x (16)	HMOS +5V 40-PIN	$17.75 NOW	HAS 8-LEVEL PRIORITY INTERRUPT CONTROLLER FOR MUXED BUS
68000	MOTOROLA	68901 MFP	10, 12.5 MHz (1M BPS)	—	—	—	4 x (8) TIMERS	NA 48-LEAD	$12.40 NOW	SINGLE-CHANNEL USART, 8-SOURCE INTERRUPT CONTROL & 8 PARALLEL I/O LINES

NA = NOT AVAILABLE
— = NOT APPLICABLE
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TABLE GROUP 3—PERIPHERAL-DEVICE CONTROLLER CHIPS

3A DISK CONTROLLERS

RELIEVE μP OF HARDWARE AND SOFTWARE OVERHEAD REQUIRED TO READ, WRITE, AND SEARCH FOR RECORDS IN PROPER DISK FORMAT. CHORES INCLUDE HEAD POSITIONING, CRC GENERATION, PROGRAM SECTOR SIZE, ETC. SEVERAL STANDARDS INCLUDING SCSI NOW APPLICABLE.

μP BUS COMPATIBILITY	SUPPLIER	PART NO	SPEED	KEY SPECIFICATIONS			TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
				COMPATIBILITY	DRIVES HANDLED	FEATURES			
32000 GENERAL	NATIONAL	DP 8466	100k BPS TO 25M BPS	ALL HARD, FLOPPY, OPTICAL DISKS	DESIGN DEPENDENT NO MAX	1. DUAL-CHANNEL DMA WITH 10M-BPS XFR 2. 48/32-BIT ECC 3. 32-BYTE FIFO 4. PROGRAMMABLE FORMAT (PATTERN & LENGTH) 5. MULTISECT COMM 6. COMPATIBLE WITH 8460/1/5/3	CMOS +5V 48-PIN 68-PIN PCC	$210 NOW	CONTROLS HARD, FLOPPY OR OPTICAL DISKS IN SINGLE OR MULTIDRIVE SYSTEMS. 8- OR 16-BIT DATA TRANSFERS. DESERIALIZES NRZ DATA. WHEN USING 8460, CONFORMS TO STD 506, SMD, ESDI & SCSI (SASI) & IPI
32000 GENERAL	NATIONAL	DP 8460 8465 8461 8462 8463	2M TO 25M BPS	ALL HARD DISKS	1	1. COMPLETE PLL 2. MFM SEPARATION 3. PREAM-LOCK IND 4. NO TRIM NEEDED 5. COMPATIBLE WITH 8466	BIPOLAR +5V 24-PIN 28-PIN PCC	$25.75 $22 NOW	8460 HAS DATA SYNCHRONIZER AND MFM SEPARATOR AND PHASE-LOCK PLL ONLY; 8465/1/2 HAVE OTHER FEATURES
32000 GENERAL	NATIONAL	DP 8464	2M TO 25M BPS	ALL HARD DISKS	1	1. ADJUSTABLE COMP HYSTERESIS 2. INPUT CAPACITOR COUPLED DIRECT TO DISK HEAD AMPLIFIER 3. IN SIG: 22-660 mV	BIPOLAR +12V 24-PIN 28-PIN PCC	$22 NOW	DISK PULSE DETECTOR ON-CHIP DIFFERENTIAL GAIN CONTROLLED AMPLIFIER, DIFFERENTIAL COMPARATOR GATING CIRCUIT, OUTPUT PULSE GENERATOR, SIGNED FOR HIGH-DENSITY DRIVES USING PLATED MEDIA & THIN-FILM HEADS
32000 GENERAL	NATIONAL	DP 8463	2M TO 25M BPS	ALL HARD DISKS	1	1. SOFT SECT ADDR MARK GEN & DETECT 2. COMPATIBLE WITH 8466/60	CMOS +5V 24-PIN 28-PIN PCC	$22 NOW	EFFICIENT CODING GIVES 30% MORE DATA FOR SAME FLUX CHANGES PER IN. REQUIRES 8462 FOR 2, 7 SYNCH AND DECODE
32000 GENERAL	NATIONAL	DP 8450 8451 8455	2M TO 25M BPS	ALL HARD DISKS	1	1. COMPLETE PLL 2. 4-BYTE PREAMBLE-LOCK INDICATION 3. COMPATIBLE WITH 8466	BIPOLAR +5V 20-PIN 20-PIN PCC	$22 NOW	8450 HAS DATA SYNCHRONIZER & PHASE-LOCK PLL ONLY. 8451/55 HAVE OTHER FEATURES. 8455 PREVENTS FALSE LOCK. 8451 PREVENTS FALSE LOCK & QUADRATURE LOCK BUT ONLY FOR HARD-SECTOR DRIVE
—	NATIONAL	DP 8470	125k–1.25M BPS	FLOPPY	1	GENERATES READ CLOCK FOR FM OR MFM ENCODED DATA	CMOS 24-PIN 28-PIN PCC	$25 2Q86	FLOPPY-DISK DATA SEPARATOR & WRITE PRECOMPENSATION, FOR NEC 765, INTEL 8272, WD 179X, NATIONAL 8466
GENERAL	NATIONAL	DP 8472 8474	125k–1.25M BPS (SOFTWARE SELECT)	FLOPPY	1, 2	INCLUDES: 1. DATA SEPARATOR 2. WRITE PRECOMP 3. MOTOR ON/OFF	CMOS 40-PIN 44-PIN PCC	$37.50 2Q86	FULL-FEATURED FLOPPY CONTROLLER INTENDED FOR EASY USE. SOFTWARE COMPATIBLE WITH NEC 765, INTEL 8272, WD 179X & NATIONAL 8466
GENERAL	WD	33C92 33C93	4M BPS	SCSI	—	IMPLEMENTS FULL SCSI PHYSICAL PATH FOR USE WITH SINGLE-ENDED INTERFACE OPTION. SUPPORTS ARBITRATION, DISCONNECT, RECONNECT, PARITY	CMOS +5V 40-PIN 44-PIN QSM 48-PIN	$25.50 NOW	SINGLE-CHIP CONVERTS FROM μP BUS TO SCSI BUS. HAS INTERNAL μP & ROM & DOES LOGICAL-TO-PHYSICAL ADDRESS TRANSLATIONS IN 150 μSEC. 33C93 HAS 48 mA DRIVERS
GENERAL	WD	5010 5020	10M BPS MFM	EDSI ST506	4	5010 IS ST-506 INTERFACE CONTROLLER, 5020 IS ESDI ADAPTOR DEVICE. 3 WAYS OF HANDLING READ ERRORS	NMOS 40-PIN 44-PIN QSM	$60 $42 NOW	WINCHESTER-DISK-CONTROLLER CHIP SET. SOFTWARE COMPATIBLE WITH 2010-05
GENERAL	WD	92C32	500k BPS	FLOPPY	1	SELF-ADJUSTING FLOPPY DATA SEPARATOR	CMOS +5V 8-PIN DIP	$5.50 NOW	PROVIDES SIGNIFICANTLY HIGHER TOLERANCE TO BIT JITTER
GENERAL	WD	16C92	—	FLOPPY	—	HANDLES PLL LOGIC, CLOCK GENERATION, WRITE PRECOMPENSATION & INTERRUPT/DMA TIMING	CMOS +5V 40-PIN	$9.50 NOW	READ/WRITE SUPPORT, COMPATIBLE WITH NEC 765A FLOPPY-DISK CONTROLLER
GENERAL	SMC	FDC 9266	8 MHz	8, 5.25, 3.5 IN.	4	BUILT-IN DIGITAL DATA SEPARATOR	NMOS 40-PIN	$12 NOW	ALL STANDARD FLOPPY-DISK SIZES
GENERAL	SMC	HDC 9224	10 MHz	ST-506 HARD DISK, FLOPPY	4	ECC, BUILT-IN DMA CONTROLLER	NMOS 40-PIN	$33.25 NOW	HARD & FLOPPY DISKS, (ALSO QIC-36 MAG TAPE)
GENERAL	SMC	HDC 9225	10 MHz	ST-506 FLOPPY	4	32k BUFFER MEMORY-MANAGEMENT UNIT	CMOS 48-PIN	$20.90 NOW	CMOS FOR LOWER POWER. COMPATIBLE WITH 9224

A sight for sore eyes.

NEC Plasma Displays cut operator fatigue and PC dimensions down to size.

The personal computer revolution faces problems, especially in offices. Eye fatigue plagues operators, while CRT displays take up ever more office space.

That's why smart OEMs are now turning to flat-panel displays. Easy-on-the-eyes NEC plasma displays rate as a top contender for several good reasons.

Our full graphic model is a mere 1.4-inch in depth, so true desktop and full-screen portable PC systems can be realized. A comparable CRT would obtrude more than 13 inches.

More important, images are clear and solid. There is no flicker, glare, distortion or blur because all dots are individually accessed and illuminated in soft neon orange. Unlike LCDs, NEC plasma displays have a very wide viewing angle—over 120 degrees. Service life is more than 30,000 hours (80,000 hours for glass alone).

Models in three formats—512 × 256-pixel, 640 × 200-pixel and 640 × 400-pixel—are available with complete driver electronics and TTL level interface. We welcome custom designs.

NEC plasma displays are also the sure way to upgrade displays for data terminals, instrumentation and test equipment. Call or write for more information today.

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NEC Building, 33-1, Shiba Gochome, Minato-ku,
Tokyo 108, Japan.
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CIRCLE NO 127

THE BEST.

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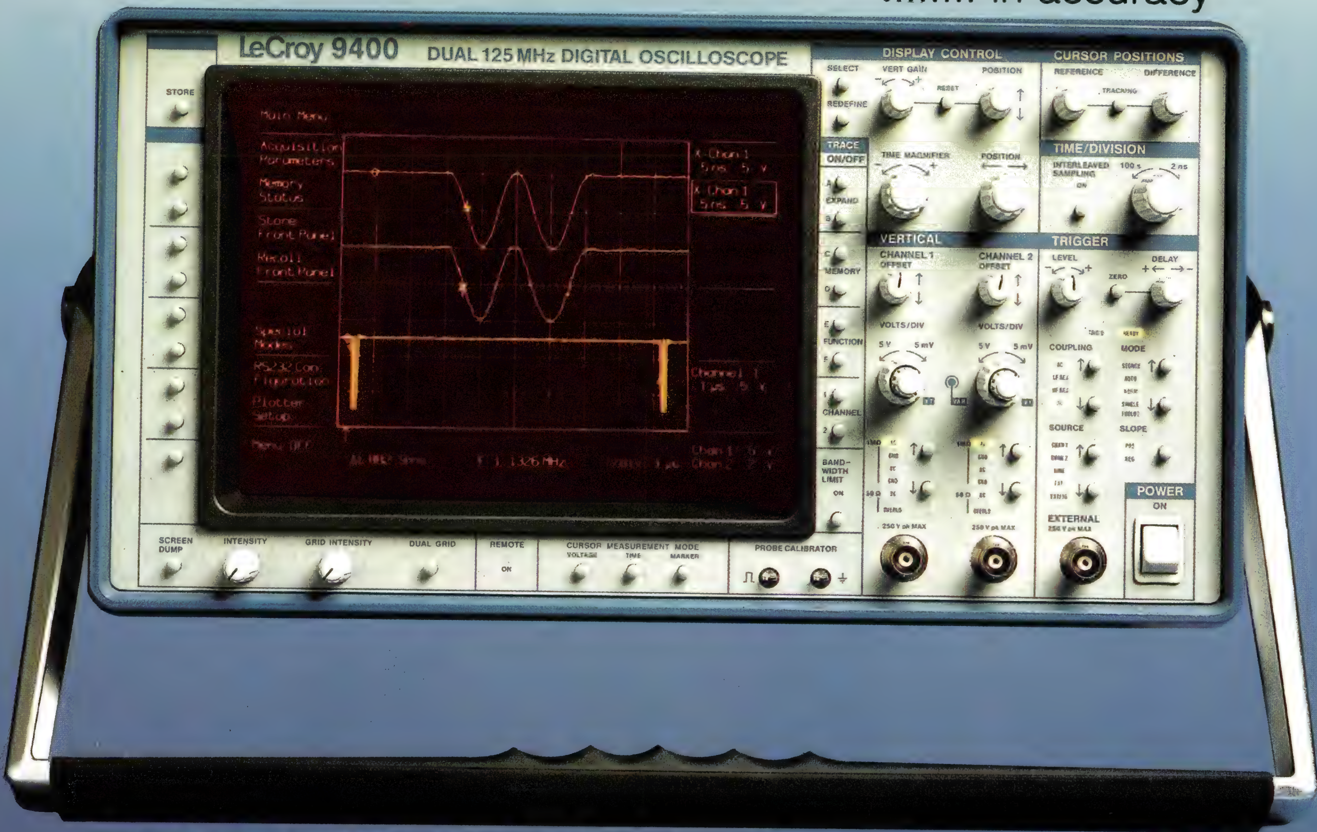


125 MHz BW; 100 MS/s ADCs; 5 GS/s Interleaved Sampling; 128 k Waveform Memory; ± 1% Accuracy; Summation and Continuous Averaging; Arithmetic Processing; Fully Programmable.

TIME RESOLUTION. Ultra-precise timing measurements — often needed in digital circuit design, lasers, radars, PCM, fiber optics, ultrasound testing — demand the LeCROY 9400's 40 psec time resolution. No other scope meets this standard, set by the 9400's *crystal-controlled time base*, uniquely precise *100 MS/s ADCs*, deep *32 k memories* per channel and sophisticated *cursor facilities*. And 32 k words/ch of memory permit *segmentation* into 8 up to 250 partitions while still maintaining horizontal resolution similar to common DSOs.

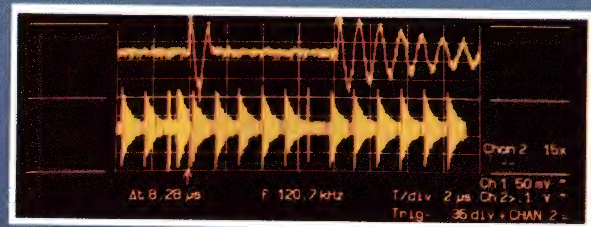
ACCURACY. Time measurements can be done with *0.002% accuracy*. The vertical accuracy of a standard 9400 is *± 2%* or optionally even *± 1%*. This means the 9400 is as much as *3 times* more accurate than any other scope today.

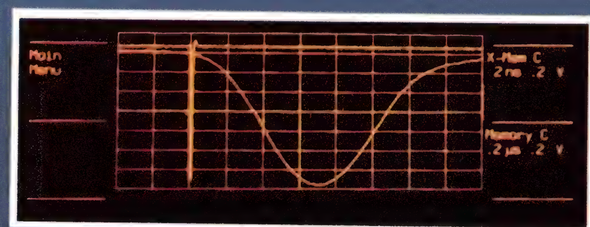
For detailed inspection of your acquired waveform, the 9400 features the exclusive *Dual Zoom* mode for up to 100 times expansion. Dual Zoom gives you two expanded traces per signal source - and when you increase the x-factor, precision and resolution improve, not deteriorate as in DSOs with shorter record lengths.

DISPLAY. The extra-high-resolution large display does full justice to the 9400's exceptional precision. *Vector graphics*, unlike raster scans, show continuous traces, finely detailed, razor sharp, without jaggies. The 1,000 × 1000 point resolution even exceeds that of a normal analog scope.

★And there is much more to say about this versatile and cost effective ($ 9900 base*) DSO. **Call us now...for details and a demonstration!!**

*USA price list only.





Top: Dual zoom and time cursors are applied to measure delay between double pulses with 100 ps resolution and 0.002% precision.

Middle: Channel 2 is segmented in 15 partitions of 2,000 words each. Expansion of event #3 appears on top.

Below: A 10 ns wide pulse is digitized with 5 Gs/s interleaved sampling speed. Expansion to 2 ns/div shows outstanding time and screen resolution.

LeCroy

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Representatives throughout the world.

Circle 48 for Demonstration

Circle 9 for Information

3A DISK CONTROLLERS *(continued)*

µP BUS COMPATIBILITY	SUPPLIER	PART NO	SPEED	KEY SPECIFICATIONS: COMPATIBILITY	DRIVES HANDLED	FEATURES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	SMC	HDC 9226	20 MHz	ST-506 HARD DISK	4	ANALOG/DIGITAL DATA SEPARATOR (SELF-ADJUSTING)	CMOS 24-PIN	$12.25 NOW	HIGH-PERFORMANCE CMOS
GENERAL	AMD	9580	NA	ST-506, ESDI	4	ON-CHIP DMA	NMOS 68-PIN	$110 2Q86	FLOPPY- OR HARD-DISK CONTROLLER
SCSI & GENERAL	MOTOROLA	68HC99	24M BPS TO DISK, 25M BYTES/SEC VIA SCSI	ST-506/412 SMD ESDI	2	73-BIT DETECT 33-BIT CORRECT TWO 522-BYTE DATA BUFFERS	HCMOS +5V 52-PIN PLCC	<$100 SAMPLES 2H86	CONTAINS 2.5-MHz 68HC11 CORE
8080/85	ROCKWELL ZILOG	6765 765A	8 MHz	5.25, 8-IN. FLOPPY	4	DUAL DENSITY, MULTIPLE SECTOR	NMOS +5V 40-PIN	$8.20 NOW $4	SIMILAR TO NEC, µPD 765A AND INTEL 8272
8080/85	ROCKWELL	6265	8 MHz	SONY 3.5-IN. FLOPPY	4	DUAL DENSITY, MULTIPLE SECTOR	NMOS +5V 40-PIN	$8.20 NOW	
68000	SIGNETICS	68454 IMDC	10 MHz 10M BPS	SA1000 ST500/506	4	COMBINED HARD- & FLOPPY-DISK CONTROLLER, SUPPORTS MFM, DATA FORMATS	NMOS +5V 48-PIN	$50 1Q86	HIGH-LEVEL COMMANDS FOR CONTROL OF HEAD AND OTHER FUNCTIONS
—	SIGNETICS	68459 DPLL	20 MHz	MFM, FM	1	20-MHz COMPOSITE DATA RATE	BIPOLAR +5V 20-PIN	$12 NOW	DISK PHASE-LOCKED LOOP FOR 68454
68000	HITACHI	63463	4, 6, 8 MHz	SMD, ST, MFM, 4 NRZ		ON-CHIP ECC & DATA BUFFER, 22 HIGH-LEVEL COMMANDS	CMOS +5V 48-PIN 52-PIN	$50 NOW	8- & 16-BIT BUS INTERFACE
GENERAL	NCR	5385E 5380 5381	10 MHz 10 MHz 10 MHz	SCSI SCSI SCSI		8-BIT PORT WITH 10 CONTROL LINES. 8-BIT PORT WITH 9 CONTROL LINES & 48-mA BUS DRIVERS. 8-BIT PORT WITH 9 CONTROL LINES & DIFFERENTIAL PAIR	NMOS +5V 48-PIN NMOS 40-PIN NMOS 48-PIN	$27.75 NOW $11.20 NOW $17.90 NOW	SCSI PROTOCOL CONTROLLER (COULD ALSO HAVE BEEN IN **TABLE 1A**, BUT PUT HERE BECAUSE SCSI OFTEN ASSOCIATED WITH DISK PERIPHERALS)

NA = NOT AVAILABLE
— = NOT APPLICABLE
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3B SERIAL TAPE CONTROLLERS

DEMAND FOR STREAMING TAPES FOR HARD-DISK BACKUP HAS CAUSED A REAWAKENING OF INTEREST IN THIS CATEGORY. INTERPRET HIGH-LEVEL READ, WRITE, AND SEARCH COMMANDS ISSUED BY µP AND GENERATE DETAILED MOTION-CONTROL SIGNALS. ALSO CONVERT PARALLEL DATA FROM µP BUS TO SERIAL FORMAT, SOMETIMES PROVIDING ERROR DETECTION. SOME INTEREST IN HAVING STANDARD BUSES LIKE SASI, SCSI, ETC.

µP BUS COMPATIBILITY	SUPPLIER	PART NO	SPEED	KEY SPECIFICATIONS: COMPATIBILITY	DRIVES HANDLED	FEATURES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	SMC G/AMI	HDC 9224	10 MHz	QIC-36 TAPE, ST-506 DISKS	4	COMPLETE MAGNETIC MEMORY CONTROLLER. BUILT-IN DMA, ECC	NMOS +5V 40-PIN CERDIP, PLASTIC, SURFACE MOUNT	$33.25 $28 NOW	CAN BE USED FOR TAPE OR DISKS. BEING USED FOR HARD-DISK BACKUP DRIVES (STREAMING TAPES)
GENERAL	WD	2401	6 MHz	SASI	—	INTERPRETS SASI HOST COMMANDS, & DOES ERROR PROCESSING, DIAGNOSTICS	NMOS +5V 40-PIN	$30 NOW	MOTION CONTROL & BUFFER MANAGER. USED WITH 24C02 R/W FORMATTER
—	WD	24C02	3.6 MHz	QIC-24	—	READ AFTER WRITE VERIFICATION. SUPPORTS 8k-BYTE BUFFER	CMOS 40-PIN	$50 NOW	READ/WRITE FORMATTER. USED WITH 2401 MOTION CONTROL. DIRECT INTERFACE TO DATA SEPARATOR

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3C CRT CONTROLLERS

ACCEPT SETUP COMMANDS FROM µP THAT DEFINE DESIRED DISPLAY (USUALLY A RASTER TYPE) AND THEN IMPLEMENT AND MAINTAIN THE DISPLAY AUTOMATICALLY. FUNCTIONS OFTEN INCLUDE FORMATTING DATA FROM µP BUS FOR VIDEO PRESENTATION TO CRT, USING CHARACTER-GENERATING CHIP IF REQUIRED. TEXT AND GRAPHIC MODES. AS WITH DISKS (**TABLE 3A**), STANDARDS ARE EMERGING.

µP BUS COMPATIBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: PROGRAMMABLE DISPLAY FORMAT	PROGRAMMABLE MONITOR FORMAT	GRAPHIC CAPABILITY	CURSOR/LIGHT PEN	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
8088 80286	PARADISE (VIA LSI LOGIC FOUNDARY)	PVC-2	14, 16 MHz CLOCK	YES	YES	YES (MONO, 16 GRAY SHADES & FULL COLOR)	YES	CMOS +5V 40-PIN	$19.50 (50k QTY) NOW	VIDEO CONTROLLER, PROVIDES MANY OF FUNCTIONS NEEDED FOR IBM PC MARKET, INCLUDING MODES FOR PLANTRONICS & HERCULES. SUPPORTS EXTERNAL COLOR SIMULATION FOR MONO

3C CRT CONTROLLERS *(continued)*

μP BUS COMPATIBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS				TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
				PROGRAMMABLE DISPLAY FORMAT	PROGRAMMABLE MONITOR FORMAT	GRAPHIC CAPABILITY	CURSOR/ LIGHT PEN			
GENERAL	TI	34061	10 MHz	YES 4096 x 4096	YES	YES	YES CURSOR	NMOS +5V 68-PIN PLCC	$31 NOW	PROVIDES EXTERNAL HOST μP WITH VIRTUALLY UNLIMITED ACCESS TO VIDEO MEMORY. CONTROLS DRAM, VIDEO RAM, & CRT
GENERAL	TI	34070	36 MHz 20 MHz	YES	YES	YES	—	NMOS +5V 22-PIN	$24 NOW $16.40 NOW	COLOR PALETTE SUPPORTS GRAPHICS SYSTEMS HAVING UP TO 4 COLOR PLANES & ALLOWS 16 OF 4096 COLORS TO BE DISPLAYED AT ONCE
GENERAL	TI	34010	50 MHz (6 MIPS)	YES 4096 x 4096 PIXEL	YES 64k x 64k	YES PixBIT	YES	CMOS +5V 68-PIN PLCC	$249 NOW	HIGH-PERFORMANCE 32-BIT μP OPTIMIZED FOR GRAPHIC DISPLAYS. HAS AN ON-CHIP INSTRUCTION CACHE & GENERAL-PURPOSE INSTRUCTION SET WITH COMPLEX FIELD MANAGEMENT
GENERAL	VTI	16160	(4 x FASTER THAN BY SOFTWARE)	—	—	YES	—	CMOS +5V 28-PIN	$16.03 NOW	HARDWARE ASSIST FOR BIT-MAPPED GRAPHICS. (ALSO IN **TABLE 1D**)
8086	NEC	82720	5 MHz	YES	YES	LINES, ARCS, ETC	YES	HMOS 40-PIN	$35 NOW	HARDWARE DRAWING ENGINE (NEC IS PRIME SOURCE)
8086 (8, 16 BITS)	INTEL	82730	8 MHz (BUS) 10 MHz (CHAR)	YES	YES	YES	YES	HMOS 68-PIN	$84.50 NOW	GRAPHICS & HIGH-PERFORMANCE TEXT MANIPULATION ON SAME DISPLAY. DMA. TABLE-DRIVEN LINKED LIST DATA STRUCTURE
8051 8096 8086	INTEL	82716 VSDD	14.5 MHz	YES	YES	YES (640 HORIZ PIXELS & 512 VERT LINES)	NO	NMOS +5V 68-PIN	$31.25 NOW	1-CHIP VIDEO STORAGE & DISPLAY DEVICE (VSDD) TARGETED AT LOW-COST TERMINALS & PERSONAL COMPUTERS (NAPLPS STD)
68000	HITACHI	63484	4, 6, 8 MHz	256 x 256 x 32	YES	4096 x 4096 BIT	2, BLOCK OR GRAPHICS	CMOS +5V 48-PIN	$55 NOW	DISPLAY FORMAT IS 256 LINE/FRAME x 256 CHAR/LINE x 32 ROW/CHAR
6800	HITACHI MOTOROLA G/AMI	6845 6845E	1–2 MHz 2–4 MHz	YES	YES	YES, CHAR	YES, BOTH	NMOS +5V 40-PIN	$2.50 $4 NOW	AN INDUSTRY STANDARD. G/AMI SAYS ITS PART HAS ADDITIONAL FEATURES
68000	MOTOROLA	68486 RMI 68487 RMC	14 MHz	YES 600 x 400 PIXELS	PAL & NTSC	YES	YES	HCMOS/ ALS 48-PIN	$56.60 (PER PAIR) NOW	CHIP SET FOR BIT-MAPPED OR OBJECT-ORIENTED SYSTEMS. OBJECT DEFINITION & MANIPULATION, COLLISION DETECTION, X/Y CAPTURE & INTERRUPT, 32 OF 4096 COLORS, VIS/VIRT SCREENS
68000	MOTOROLA	68490 RGDP	12.5–16 MHz	YES	YES	VECTOR	—	CMOS +5V 124-PIN PGA	NA 1987	SUPPORTS 4k x 4k VRAM FRAME BUFFER, 8 BITS PER PIXEL. VDI/CGI SOFTWARE AVAILABLE (GSS, $175). HIGH-PERFORMANCE RASTER & VECTOR FUNCTIONS TO ANSI STANDARD
6502 6800 68000	ROCKWELL	6545 65C45	3.7 MHz 2–8 MHz	YES	YES	YES, CHAR	YES, BOTH	NMOS +5V CMOS 40-PIN	$5.50 NOW	PIN COMPATIBLE WITH 6845. TRANSPARENT ADDR INTERLACE, DRAM REFRESH
68000 6502 8085 Z80	ROCKWELL	6549	28 MHz	YES	YES	YES	NO	NMOS +5V 40-PIN	$32 NOW	HI-END VIDEO GEN: FULL VIDEOTEX (VTX), TELETEX (TTX) GRAPHICS. DRAM INTERFACE. 4096 COLOR. N AMER PRESENTATION LEVEL PROTOCOL SYNTAX (NAPLPS). RGB OUTPUTS
GENERAL	AMD	8052	4, 6, 8 MHz	YES	YES	TEXT ONLY	CURSOR	NMOS 68-PIN	$35 NOW	FOR ALPHANUMERIC USE. SUPPORTS UP TO 132 CHARACTERS, SPLIT-SCREEN SOFT SCROLL, WINDOWING & CHARACTER ATTRIBUTES. ON-CHIP DMA
GENERAL	AMD	8152A	45, 80 MHz	—	—	—	—	BIPOLAR 48-PIN	$12 NOW	VIDEO-SYSTEM CONTROLLER, SUPPORTS CHARACTER ATTRIBUTES & OUTPUTS VIDEO IN ANALOG OR DIGITAL
GENERAL	AMD	8150 8150A	40 MHz 50 MHz	YES YES	YES YES	— —	— —	BIPOLAR 48-PIN BIPOLAR 48-PIN	$45 NOW $28 2Q86	DISPLAY REFRESH CONTROLLER. SUPPORTS MEMORY REFRESH, VIDEO REFRESH & MEMORY ARBITRATION. 8150A SUPPORTS VRAMs & DRAMs
GENERAL	AMD	8151	200 MHz	—	YES	—	—	BIPOLAR 40-PIN	$64 NOW	GRAPHICS COLOR PALETTE. 256 x 8 COLOR MAP PLUS DAC FOR ECL/TTL SYSTEMS
GENERAL	AMD	8157 8177	125 MHz 200 MHz	— —	— —	— —	— —	BIPOLAR 40-PIN BIPOLAR 24-PIN	$24 NOW $14 NOW	VIDEO SHIFT REGISTER (16-BIT, 20-BIT) WITH READBACK. VIDEO DATA SERIALIZER (16-BIT) TTL IN, ECL OUT
GENERAL	AMD	8158	125 MHz	YES	YES	—	—	BIPOLAR 28-PIN	$34.60 NOW	VIDEO TIMING CONTROLLER PROVIDES SYNCH & TIMING SIGNALS
GENERAL	AMD	8159	63 MHz	—	YES	—	—	BIPOLAR 48-PIN	$42.65 2Q86	3-GUN COLOR PALETTE. COLOR MAP 64 x 13 PLUS 3 DACs

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Both boards offer Multithreaded I/O. Which means you can run up to four drives concurrently with true overlapped operation. You can even upgrade from ST506 to SMD without having to rewrite your I/O driver.

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Of course, we should warn you that someday someone will build controllers even faster than these.

In fact, we're already working on them.

adaptec

CIRCLE NO 130

3C CRT CONTROLLERS *(continued)*

μP BUS COMPATIBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: PROGRAMMABLE DISPLAY FORMAT	PROGRAMMABLE MONITOR FORMAT	GRAPHIC CAPABILITY	CURSOR/LIGHT PEN	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	AMD	8171 8172	75 MHz 200 MHz	— —	— —	— —	— —	BIROLAR 24-PIN BIPOLAR 24-PIN	$24 3Q86 $40 3Q86	VIDEO DATA ASSEMBLY FIFO (TTL) SUPPORTS PANNING & HARDWARE WINDOWING
—	AMD	95C60	20 MHz	YES	YES	YES	YES	CMOS 144-PIN	$160 4Q86	QUAD PIXEL DATA FLOW (QDPM) GENERATES TEXT & GRAPHICS. DRAWS VECTORS, CIRCLES, LINES. SUPPORTS GKS, NAPLPS. CASCADABLE & HANDLES 4k x 4k MEMORY OR 4k x 2k
8048 8080 8086	NATIONAL	NS 405 455 (TMP)	12–18 MHz	YES	YES	YES	YES	NMOS +5V 48-PIN	$24.20 NOW	1-CHIP μC 8048 CORE ENHANCED SO THAT IT CONTAINS MOST OF FUNCTIONS NEEDED FOR CRT TERMINAL

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

3D KEYBOARD AND/OR DISPLAY INTERFACES

UNBURDEN THE MAIN μP FROM THE TIME-CONSUMING TASKS OF SCANNING KEYS, EXCITING DISPLAYS, AND PERFORMING THE NECESSARY CODE CONVERSION. ALSO HELPFUL FOR CUTTING DOWN CABLE COMPLEXITY IN MODULAR KEYBOARDS AND DISPLAYS.

μP BUS COMPATIBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: NUMBER OF KEYS	DISPLAY BIT PATTERNS	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	SUPERTEX	HV01 HV02	6 MHz	—	16 LINES PER CHIP EL OR PLASMA, DOT MATRIX, CASCADABLE	HVCMOS (CMOS + DMOS) 36-PIN	$49.09 NOW $34.48 NOW	HV01 IS 0–60V, 16-CHANNEL GRAY SHADE COLUMN DRIVER, HV02 IS 250V, 16-CHANNEL ROW DRIVER
GENERAL	SUPERTEX	HV03/ HV05, HV04/ HV06	8 MHz	—	64 LINES PER CHIP EL OR PLASMA, DOT MATRIX, CASCADABLE	HVCMOS (CMOS + DMOS) 36-PIN	$23.79 $42.42 $23.79 $42.42 NOW	HV03/05 IS 64-CHANNEL 90V COLUMN DRIVER. HV04/06 IS 64-CHANNEL 300V ROW DRIVER
GENERAL (SERIAL)	MOTOROLA	MC 145000 (MASTER) 145001 (SLAVE)	250-Hz MAX DISPLAY FREQ	—	48 LCD SEGMENTS DRIVEN BY MASTER & 44 ADDITIONAL LCD SEGMENTS BY EACH SLAVE	CMOS 3–6V 24-PIN 18-PIN	$7.32 NOW $6.50 NOW	SERIAL I/O. MASTER DRIVES 12 FRONT & 4 BACKPLANES FOR 48 SEGMENTS. SLAVE DRIVES 44 ADDITIONAL FRONT PLANES
GENERAL (SERIAL)	MOTOROLA	MC 14499	—	—	4 x 7-SEGMENT LED CHARACTERS WITH DECIMAL POINT	CMOS 4.5–6.5V 18-PIN	$2.50 NOW	SERIAL INTERFACE
GENERAL (SERIAL)	MOTOROLA	MC 145453	—	—	33 LCD SEGMENTS, BARS OR DOTS. MAY PARALLEL MORE DEVICES TO INCREASE SEGMENTS	CMOS 3–10V 40-PIN	$4.17 1Q86	SERIAL INTERFACE
GENERAL (SERIAL DATA + 4 CONTROL LINES)	G/AMI	S 4520A 4520B	2 MHz CLOCK IN	—	FOR DRIVING HIGH-VOLTAGE DICHROIC LCDs UNDER μP CONTROL. 38 SEGMENTS PLUS BACKPLANE CASCADABLE USING 4520A & 4520Bs. ON-CHIP OSC FOR GENERATING BACKPLANE AC	CMOS 3–16V (32V) 48-PIN 44-PIN PLCC 48-PIN CLCC	NA NOW	DRIVER FOR LIQUID-CRYSTAL & FLAT-PANEL DISPLAYS & ALSO PRINT HEADS
GENERAL	OKI	5219B	1 MHz	—	48-DOT STATIC DRIVER	CMOS +5V	$4.25 NOW	
GENERAL	OKI	5839B	8 MHz	—	32-DOT ROW DRIVER	CMOS +5V	$3.95 NOW	6222 IS CONTROLLER
GENERAL	OKI	5260	8 MHz	—	80-DOT ROW/COLUMN DRIVER	CMOS +5V	$5.50 NOW	
GENERAL	OKI	6222	380 kHz	—	16-DOT OR 40-COLUMN DRIVER/CONTROLLER	CMOS +5V	$6.25 NOW	
GENERAL	OKI	6255	11 MHz	—	DOT-MATRIX CONTROLLER	CMOS +5V	$9.50 NOW	DUTY CYCLE 1/2 TO 1/250
GENERAL	OKI	6265	11 MHz	—	DOT-MATRIX CONTROLLER	CMOS +5V	$15.50 NOW	HD6845 SOFTWARE COMPATIBLE 1/100 DUTY CYCLE
GENERAL	SMC	KR 9600-005	100 kHz	90	—	NMOS +5V 40-PIN	$7.30 NOW	PIN COMPATIBLE WITH KR3600, STD ASCII CODE
GENERAL	SMC	KR 9601-012	4 MHz	90	—	NMOS +5V 40-PIN	$7.30 NOW	ASCII CODE OUT, CAPS LOCK & AUTOREPEAT
GENERAL	SMC	KR 9602-005	4 MHz	90	—	NMOS +5V 28-PIN	$7.30 NOW	ASCII CODES SERIAL OUT, CAPS LOCK & AUTOREPEAT
GENERAL	INTERSIL	7211 7212	—	—	4-DIGIT, 7-SEG BCD INPUT, DECODED DIRECT-DRIVE OUTPUT	CMOS 40-PIN	$2.50 NOW	7211 IS LCD DRIVER. 7212 IS LED DRIVER

3D KEYBOARD AND/OR DISPLAY INTERFACES *(continued)*

µP BUS COMPATIBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: NUMBER OF KEYS	KEY SPECIFICATIONS: DISPLAY BIT PATTERNS	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	INTERSIL	7218	—	—	8-DIGIT, 7-SEG COMMON CATHODE OR COMMON ANODE LED, 8 x 8 RAM. CAN POWER DOWN TO 2V & RETAIN DATA	CMOS 28-PIN	$5.66 NOW	DIGIT & SEGMENT DRIVERS. MUX SCAN, DIRECT µP INTERFACE
GENERAL	INTERSIL	723X	—	—	4 TO 10½ CHAR, 7 TO 16 SEG, ALPHANUMERIC LCD DRIVERS, FLAGS	CMOS 40-PIN	$5.25 NOW	SERIAL, PARALLEL & ASCII INPUT. CASCADABLE, AUTOSCROLL
GENERAL	INTERSIL	7280 7281 7283	—	—	LCD DOT-MATRIX CONTROLLER/DRIVERS, CHAR FONT UP TO 6 x 10 DOTS, 120 CHAR RAM, 4 USER-DEFINED CHARS	CMOS 40-PIN	$5 NOW	DIRECT µP INTERFACE, FULLY CASCADABLE, MUXED PARALLEL BUS
GENERAL	INTERSIL	7243	—	—	8 CHAR x 14 OR 16 SEG, ALPHANUMERIC	CMOS 40-PIN	$7 NOW	MUXED LED DRIVER, 6-BIT PARALLEL ASCII INPUT, FULLY CASCADABLE

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

3E LAN CONTROLLERS

LAN (LOCAL-AREA-NETWORK) CONTROLLERS PROVIDE THE PROTOCOL MANAGEMENT FOR THE INTERCONNECTION OF COMPUTERS AT FAIRLY HIGH SPEEDS AND AT DISTANCES OF ABOUT A MILE. COLLISION-DETECTION AND TOKEN-PASSING SCHEMES AS WELL AS OTHERS ARE INCLUDED. SEE ALSO **TABLE 1B.**

µP BUS COMPATIBILITY	SUPPLIER	MODEL	BUS SPEED	KEY SPECIFICATIONS: LAN LINK SPEED	KEY SPECIFICATIONS: OTHER FEATURES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL 16-BIT	AMD (MOSTEK)	7990 (LANCE) 68591	—	10M BPS	IEEE 802.3 ETHERNET LAN SPECS. DMA TO 24-BIT ADDRESS SPACE	NMOS +5V 48-PIN	$64 NOW	ETHERNET, CHEAPERNET CONTROLLER; WORKS WITH 7992 SERIAL CHIP & 7996 TRANSCEIVER. MOSTEK IS QUESTIONABLE SOURCE
ETHERNET CHEAPERNET (SERIAL)	AMD MOSTEK	7992B (SIA) 68591	—	10M BPS	IEEE 802.3 ETHERNET LAN MANCHESTER ENCODER/DECODER. GUARANTEED −275 & −175-mV CARRIER DETECTION LIMITS	BIPOLAR +5V 24-PIN	$19.15 NOW	ETHERNET SERIAL INTERFACE ADAPTER (SIA). TO WORK WITH 7990 CONTROLLER. MOSTEK IS QUESTIONABLE SOURCE
ETHERNET CHEAPERNET (SERIAL)	AMD	7996	—	10M BPS	IEEE 802.3 ETHERNET LAN SPECS. CSMA/CD WITH JABBER CONTROLLER & SQE TEST	BIPOLAR 20-PIN	$23.90 NOW	ETHERNET, CHEAPERNET TRANSCEIVER. WORKS WITH 7990 & 7992
GENERAL	AMD	7960	—	0.5M–3M BPS	FOR DRIVING VIA ISOLATION TRANSFORMER WITH MODEM-LIKE INTERFACE. 32-dB DYNAMIC RANGE	BIPOLAR 24-PIN	$13.65 NOW	UNIVERSAL NETWORK TRANSCEIVER (FOR LOW-SPEED NETWORKING)
68000 (16 OR 8 BIT)	ROCKWELL	68802	—	1M–10M BPS	IEEE 802.3 ETHERNET S-LAN. 32-BYTE BUFFER MANAGEMENT, DMA & PROGRAMMABLE 2- OR 6-BYTE ADDRESS RECOGNITION	NMOS +5V 40-PIN	$36 2Q86	UNIVERSAL 802.3 LAN CONTROLLER, FOR IBM-PC, ETHERNET & S-LAN. CAN RUN SLOWER TO REDUCE CABLING COSTS
8086/88 80186/88 80286	INTEL	82586	4M BYTES/SEC DMA	100k BPS TO 10M BPS	IEEE 802.3, WITH PROGRAMMABLE PARAMETERS, BUS MASTER. CAN INTERFACE AS COPROCESSOR TO 80186/88 µPs	HMOS II +5V 48-PIN	$71 NOW	SAID TO BE ONLY LAN CONTROLLER THAT SUPPORTS ETHERNET, CHEAPERNET, IBM PC NETWORK, STARLAN BASE & BROADBAND
—	INTEL	82501	NA	10M BPS	SERIAL INTERFACE TO IEEE 802.3 (ETHERNET) CABLE	BIPOLAR +5V 20-PIN	$38.50 NOW	MANCHESTER ENCODER/DECODER FOR 82586 LAN CONTROLLER
—	INTEL	82C502	NA	10M BPS	ETHERNET/CHEAPERNET TRANSCEIVER CONFORMING TO IEEE 802.3. CAN DRIVE 50M CABLE	CMOS +5, +10V 16-PIN	$38.50 NOW	PROVIDES TRANSMIT, RECEIVE & COLLISION DETECT. PART OF 82586, 82501 CHIP SET
GENERAL	INTEL	82588	NA	100k BPS TO 5M BPS	LOWER-SPEED IEEE 802.3 CONTROLLER WITH NRZI & MANCHESTER ENCODER/DECODER (2M BPS) ON CHIP WITH COLLISION DETECTION	HMOS II +5V 28-PIN	$50 NOW	SUPPORTS IBM PC NETWORK, STARLAN (IEEE 802.3). INTERFACES DIRECTLY TO 80186/88 µPs
GENERAL (VIA FIFO)	INTEL	8044 8344	12 MHz	2.4M BPS (EXTERNAL CLOCK)	4k x 8 ROM, 192 x 8 RAM, 4 x (8) PORTS & 2 x (16) TIMERS. 0 ROM	HMOS II +5V 40-PIN	$21.50 1k QTY $22.20 NOW	IS 8051 µC WITH ON-CHIP SDLC CONTROLLER 8344 IS ROMLESS VERSION
GENERAL	NATIONAL	DP 8390 NIC	NA	1M–10M BPS	IEEE 802.3 CONTROLLER	CMOS +5V 48-PIN	$50 NOW	3-CHIP SET FOR ETHERNET OR CHEAPERNET
ETHERNET	NATIONAL	DP 8391 SNI	—	1M–10M BPS	IEEE 802.3 ENCODER/DECODER	BIPOLAR 24-PIN	$25 NOW	DIGITAL PLL WITH HIGH JITTER TOLERANCE
ETHERNET	NATIONAL	DP 8392 CTI	—	1M–10M BPS	IEEE 802.3 TRANSCEIVER	BIPOLAR 16-PIN	$26 NOW	SINGLE-CHIP TRANSCEIVER FOR ETHERNET/CHEAPERNET

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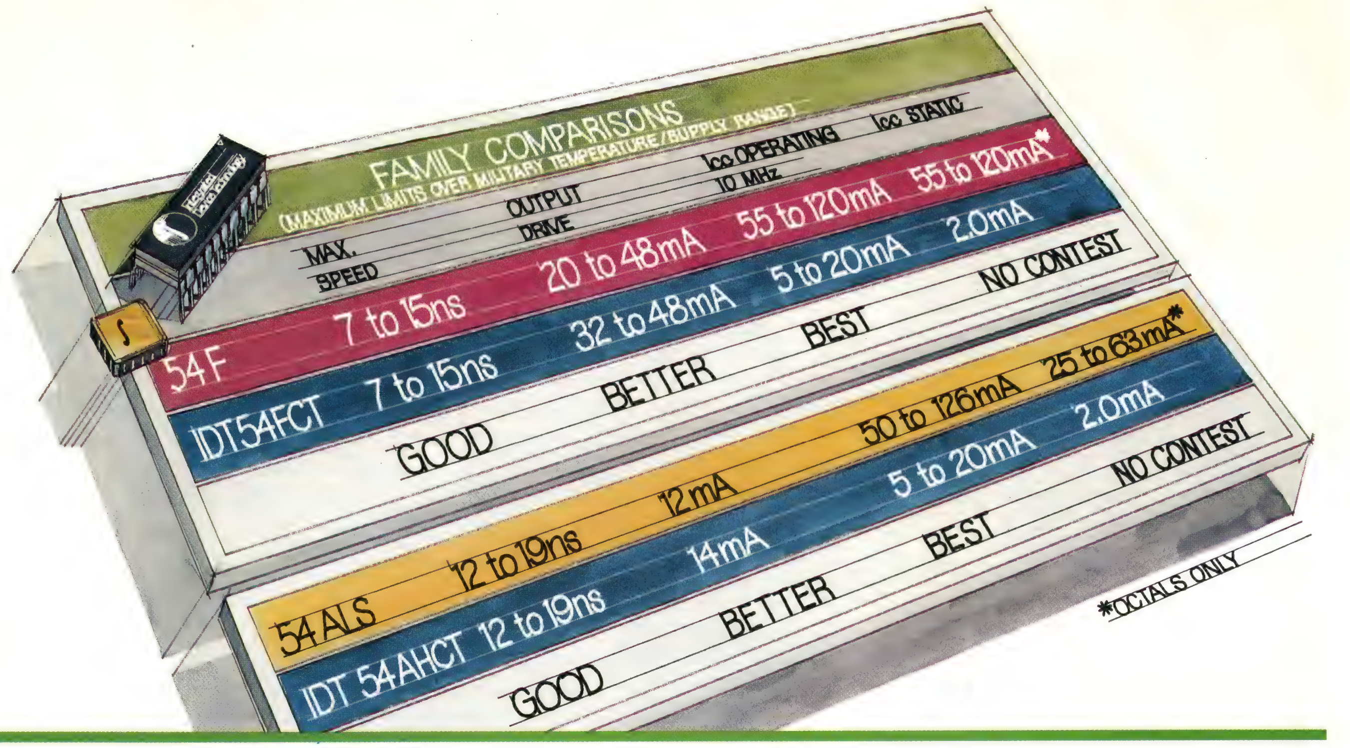

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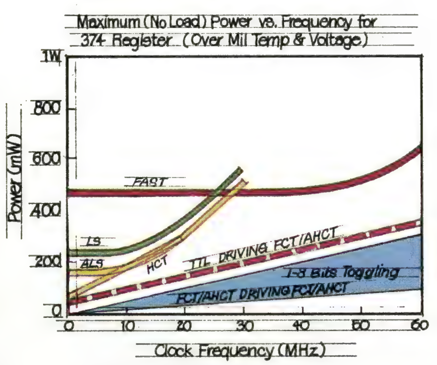

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This unique combination of speed and output drive with low power is achieved with our advanced, stepper aligned, dry etched CEMOS™ II process.

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☐ **Inputs.** 5μA max input current levels are substantially lower than bipolar.

☐ **Outputs.**
Com'l FCT = 48–64mA
Mil FCT = 32–48mA
Com'l AHCT = 24mA
Mil AHCT = 12mA

IDT54/74 FCT and AHCT	Introduction
Registers	
574	Now
374	Now
273	Now
299	Now
377	Now
534	Now
Latches	
573	Now
373	Now
533	Now
Buffers	
240	Now
244	Now
Transceivers	
245	Now
645	Now
640	Now
Decoders	
138	Now
139	Now
Comparators	
521	Now
Carry look ahead generators	
182	Now

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3E LAN CONTROLLERS *(continued)*

µP BUS COMPATIBILITY	SUPPLIER	MODEL	BUS SPEED	KEY SPECIFICATIONS: LAN LINK SPEED	KEY SPECIFICATIONS: OTHER FEATURES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL 68000 8086 (8 & 16 BIT)	TI	38010 38020 38030 38051 38052	5M BPS	4M BPS	IEEE 802.5 TOKEN-PASSING RING, HANDLES ALL LAN ADAPTER FUNCTIONS, INCLUDING MEDIA ATTACH (TWISTED PAIR), BUFFERING & MANAGEMENT, PROTOCOL PASSING, & ATTACHING SYSTEM INTERFACE	NMOS +5V 48-PIN NMOS +5V 48-PIN NMOS +5V 100-PIN BIPOLAR +5V 22-PIN BIPOLAR +5V 20-PIN	$125 PER 5-CHIP SET, 50k QTY	DEVICES FOR TOKEN-PASSING-TYPE LAN DEVELOPED WITH IBM TO IBM SPECS, WHICH WERE SAID TO BE BASIS FOR IEEE 802.5 STANDARD
68000 GENERAL (8 & 16 BITS)	MOTOROLA	68824 TBC	10, 12.5 MHz	1M, 5M, & 10M BPS	IEEE 802.4 MEDIA ACCESS CONTROL, WHICH MAP SPECIFIES AS LAYER 2. PERFORMS FRAME FORMATTING & TOKEN MANAGEMENT. INCLUDES 4 DMA CHANNELS & 40-BYTE FIFO	CMOS 84-PIN PGA	$75.95 NOW	TOKEN BUS CONTROLLER FOR MAP (MANUFACTURING AUTOMATION PROTOCOL) SPONSORED BY GM & BOEING
(MAP)	MOTOROLA	68184 BIC	—	10M BPS	BROADBAND INTERFACE CONTROL CHIP (BIC). CONNECTS TO 68824 TBC. SCRAMBLES/DESCRAMBLES DATA. INSERTS/DELETES KICKER	(MACROCELL ARRAY) 44-PIN	NA 1Q86	MACROCELL ARRAY IMPLEMENTATION OF DIGITAL PORTION OF IEEE 802.4 BROADBAND PHYSICAL LAYER
(MAP)	MOTOROLA	68194 CBM	—	10M BPS	CARRIER MODEM CHIP (CBM), INTERFACES TO 68824 TBC FOR SINGLE-CHANNEL CARRIER NETWORK	BIPOLAR 144-PIN	NA 4Q86	IEEE 802.4 PHASE-COHERENT CARRIER PHYSICAL LAYER. MODULATOR/DEMODULATOR
GENERAL & MAP	G/AMI	DATA CHIP DMA CHIP PROTOCOL CHIP		10M BPS	3-CHIP SET FOR MAP FACTORY AUTOMATION (IEEE 802.4) NETWORK	CMOS CMOS CMOS	NA NA NA 3Q86	STARTED OUT AS CUSTOM CONVERSION OF 3 CONCORD DATA SYSTEM BOARDS. CDS SCHEDULED TO RECEIVE FIRST SAMPLES 1Q86
GENERAL (8-BIT)	SMC	COM 9026	5 MHz	2.5 BPS	ARCNET (DATAPOINT) CONTROLLER	NMOS +5V 40-PIN	$32.80 NOW	CONTROLLER FOR TOKEN-PASS LOCAL-AREA NETWORK. 9032 IS COMPANION CHIP
ARCNET	SMC	COM 9032	—	2.5M BPS	ARCNET (DATAPOINT) COMPATIBLE TRANSCEIVER	NMOS +5V 16-PIN	$16.85 NOW	ENCODES & DECODES ARCNET "DIPULSES" FOR LAN CABLE AMPLIFIERS. USED WITH 9026 CONTROLLER
ARCNET	SMC	HYC 9058	—	2.5M BPS	ARCNET (DATAPOINT) HYBRID LINE DRIVER. ALLOWS BUS CONFIGURATION OF ARCNET LANs	HYBRID NA	$45 1Q86	DRIVES COAX LINE. COMPATIBLE WITH EXISTING ZENITH LANB. DESIGNATED HIT (HI IMPEDANCE TRANSCEIVER)

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

3F POWER DRIVERS AND CONTROLLERS

MANY OF THESE DEVICES CAN DRIVE THE INDUCTIVE LOADS OF ELECTROMECHANICAL MACHINERY. A NEW EMPHASIS IS TO MAKE THEM SMART, INCORPORATING SELF-CONTROL AND THE ABILITY TO FEED BACK INFORMATION TO HOST µP, ETC.

µP BUS COMPATIBILITY	SUPPLIER	MODEL	BUS SPEED	KEY SPECIFICATIONS: OUTPUT SPEED	KEY SPECIFICATIONS: OTHER FEATURES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	SILICONIX	D-469	—	100 nSEC PROP DELAY	500-mA SOURCE & SINK OUTPUTS (2% DUTY CYCLE). TTL LOGIC INPUTS	CMOS +5 +14V 14-PIN	$2.92 NOW	QUAD MOSPOWER DRIVER, INVERT & NONINVERT INPUTS. LOW ON RESIST OUTPUTS
GENERAL	SPRAGUE	ULN-2000A SERIES	—	—	TO 500 mA, TO 95V	BIPOLAR 16-PIN	$0.57–$0.81 NOW	INDUSTRY-STANDARDS, 7 DARLINGTON DRIVERS WITH TRANSIENT SUPPRESS
GENERAL	SPRAGUE	UCN-5800A	5 MHz	—	350 mA, 50V	BIMOS 14-PIN	$0.99 NOW	4-BIT LATCHED DRIVER WITH TRANSIENT SUPPRESS
GENERAL	SPRAGUE	UCN-5801A	5 MHz	—	350 mA, 50V	BIMOS 22-PIN	$1.81 NOW	8-BIT LATCHED DRIVER WITH TRANSIENT SUPPRESS
GENERAL	SPRAGUE	UCN-5810A	5 MHz	—	−25 mA, 60V	BIMOS 18-PIN	$1.56 NOW	10-BIT SERIAL IN, LATCHED SOURCE DRIVER
GENERAL	SPRAGUE	UCN-5815A	2 MHz	—	−25 mA, 60V	BIMOS 22-PIN	$1.95 NOW	8-BIT LATCHED SOURCE DRIVER
GENERAL	SPRAGUE	UCN-5826B	5 MHz	—	1.75A, 80V	BIMOS 18-PIN	$2.98 NOW	4-BIT SERIAL IN, LATCHED DRIVER WITH TRANSIENT SUPPRESS
GENERAL	SPRAGUE	UCN-5832A	5 MHz	—	100 mA, 40V	BIMOS 40-PIN	$4.34 NOW	32-BIT SERIAL IN, LATCHED DRIVER, LOW SATURATION V
GENERAL	SPRAGUE	UCN-5890A	5 MHz	—	−350 mA, 80V	BIMOS 16-PIN	$2.22 NOW	8-BIT SERIAL IN, LATCHED SOURCE DRIVER WITH TRANSIENT SUPPRESS
GENERAL	SPRAGUE	UCN-5895A	5 MHz	—	−120 mA, 50V	BIMOS 16-PIN	$2.16 NOW	8-BIT SERIAL IN, LATCHED SOURCE DRIVER, LOW SATURATION VOLTAGE
GENERAL	SPRAGUE	UDN-2933B	—	—	±0.8A, 30V	BIPOLAR 16-PIN	$1.85 NOW	3-CHANNEL FULL-BRIDGE MOTOR DRIVER WITH TRANSIENT SUPPRESS

3F POWER DRIVERS AND CONTROLLERS *(continued)*

μP BUS COMPAT-IBILITY	SUPPLIER	MODEL	BUS SPEED	KEY SPECIFICATIONS: OUTPUT SPEED	KEY SPECIFICATIONS: OTHER FEATURES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	SPRAGUE	UDN-2941B	—	—	−1.5A, 35V	BIPOLAR 16-PIN	$2.70 2Q86	QUAD SOURCE DRIVER WITH TRANSIENT SUPPRESS
GENERAL	SPRAGUE	UDN-2953B	—	—	±2A, 50V	BIPOLAR 12-PIN SIP	$2.30 NOW	FULL-BRIDGE MOTOR DRIVER, PWM CURRENT CONTROL
GENERAL	SPRAGUE	UDN-2965W	—	—	±0.4A, 60V	BIPOLAR 16-PIN SIP	$5.07 1Q86	DUAL SOLENOID MOTOR DRIVER, PWM CURRENT CONTROL
GENERAL	SPRAGUE	UDN-2993B	—	—	±0.5A, 40V	BIPOLAR 16-PIN	$1.70 NOW	DUAL FULL-BRIDGE MOTOR DRIVER WITH TRANSIENT SUPPRESS
"C-BUS" (3-LINE SERIAL)	SIGNETICS	TEA 1017	50 kHz	—	13 PUSH-PULL OUTPUTS, 80 mA BIDIRECTIONAL EACH, WITH CLAMPING DIODES. CAN BE PAIRED FOR MORE CURRENT	BIPOLAR 5–18V 18-PIN	$2.02 NOW	13-BIT SERIAL TO PARALLEL CONVERTER FOR DRIVING LEDs, TRIACs, RELAYS, AND STEPPER MOTORS
GENERAL	SIEMENS	SMT-12	—	<5 μSEC SWITCH	TO HANDLE 50V, 250 mA, WITH 12A SHORT CIRCUIT RATING	CMOS + DMOS, 5-PIN TO-220	$30 EA, SAMPLES 1Q86, PROD IN 87	POWER DEVICE WITH LOGIC TO SIGNAL μP WHETHER SHORTED, OPENED, ETC VIA EXTRA FEEDBACK PIN
GENERAL (8-BIT)	TI	2000	10 MHz	—	16-BIT UP/DOWN COUNTER. DIRECTION DISCRIMINATOR, FREQ OR PULSE-DUR MEASUREMENT	CMOS +5V 28-PIN	NA NA	FOR MOTOR CONTROLS: DIRECTION, RATE, POSITION MONITORING, ETC
GENERAL (8-BIT)	NATIONAL	LM628 629	NA	256 μSEC SAMPLING RATE (100k+ RPM)	INTERNAL DEDICATED μP EXECUTES PID COMPENSATION ALGORITHM, USING 32-BIT ALU, 16 x 16 = 32 MULTIPLY (7 μSEC), AND ALGORITHM FIRMWARE	NMOS +5V 28-PIN	NA '86	DC-MOTOR POSITION CONTROL SERVO THAT ACCEPTS POSITION COMMANDS FROM HOST μP. COMPUTES TRAPEZOIDAL TRAJECTORY

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

TABLE 4—μPs AND μP-LIKE CHIPS

THE ULTIMATE IN FLEXIBLE, POTENTIALLY INTELLIGENT PERIPHERAL CONTROLLERS, THESE DEVICES ARE 1-CHIP μPs MODIFIED TO SERVE AS SLAVES OF THE MAIN μP. SOFTWARE PREPARATION FOR THEM CAN BE EASIER FOR THESE CONTROLLERS THAN FOR THE MAIN μPs BECAUSE IN THIS CASE THE SOFTWARE REMAINS ISOLATED FROM THE MAIN SYSTEM SOFTWARE. SOME OF THESE DEVICES NOW SELL FOR $1 OR LESS IN HIGH (100k) VOLUMES. BUT THESE DEVICES USUALLY SUFFER IN SPEED COMPARED WITH THE DEDICATED SOLUTIONS LISTED ELSEWHERE IN DIRECTORY. SEE EDN μP/μC DIRECTORY (NOVEMBER 28, 1985, PG 106) FOR MORE COMPLETE DESCRIPTION.

μP BUS COMPAT-IBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: ROM	KEY SPECIFICATIONS: RAM	KEY SPECIFICATIONS: PORT BITS	KEY SPECIFICATIONS: TIMER BITS	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL (4-BIT, 8-BIT, SERIAL)	NATIONAL	COP413L	4 MHz	0.5k x (8)	32 x (4)	16	—	NMOS 20-PIN	$1.26 (1k) NOW	FAMILY OF 4-BIT μCs THAT HAS MANY VARIATIONS; THESE ARE JUST A SAMPLE. THE 438N HAS 8-CHANNEL A/D
		COP413C		0.5k x (8)	32 x (4)	16	—	CMOS 20-PIN	$2.30 (1k) NOW	
		COP484		4k x (8)	NA	23	YES	NMOS 28-PIN	NA 2Q86	
		COP438N		0	64 x (4)	—	—	CMOS 20-PIN	$6.75 (1k) NOW	
GENERAL	INTEL AMD	8051 80C51 8751 9761	12 MHz 16 MHz 12 MHz 12 MHz	4k x (8) 4k x (8) 4k x (8) 8k x (8)	128 x (8) 128 x (8) 128 x (8) 128 x (8)	4 x (8) 4 x (8) 4 x (8) 4 x (8)	2 x (16) 2 x (16) 2 x (16) 2 x (16)	NMOS CMOS NMOS NMOS 40-PIN	$6.70 $11.20 $43 $53 NOW	A POPULAR CONTROLLER μC, IT IS WIDELY SECOND SOURCED. NEW 16 MHz 80C51 HAS 500k BPS SERIAL PORT
GENERAL	ZILOG	Z8 SUPER8	1–3 μSEC CYCLE	2k x (8) 4k x (8) 4k x (8)	256 x (8) 356 x (8)	4 x (8) 4 x (8)	2 x (8)	NMOS 40-PIN CMOS 48-PIN	$5 NOW $10 NOW	ARCHITECTURE FEATURES A LARGE NUMBER OF GENERAL-PURPOSE REGISTERS IN CPU RAM
6800	MOTOROLA	3870	1 MHz	2k x (8)	64 x (8)	32	1 x (8)	NMOS 40-PIN	$7 (5k MIN) NOW	ORIGINAL SOURCES MOSTEK & FAIRCHILD HAVE BECOME QUESTIONABLE
6800	MOTOROLA	6805S3	1 MHz	3.7 x (8)	104 x (8)	20, 1	2 x (8) 1 x (16) (WATCH-DOG)	NMOS 28-PIN	NA NOW	6805S2 WITH EXTRA MEMORY & EXTRA TIMER. PRICES FOR FAMILY RANGE FROM $0.50 TO $40
6800	MOTOROLA	68HC805C4	2 MHz	4k x (8) EEPROM	176 x (8)	32	1 x (16)	CMOS 40-PIN 44-PIN PLCC	$150 (OR LESS) 1Q86	EEPROM VERSION OF 68HC05C4
6800	MOTOROLA	68HC811A2	2.1 MHz	2k x (8) EEPROM	256 x (8)	41	1 x (16)	CMOS 40-PIN 52-PIN PLCC	$175 (OR LESS) 1Q86	HAS 2 SERIAL PORTS, A/D & ENHANCED TIMER

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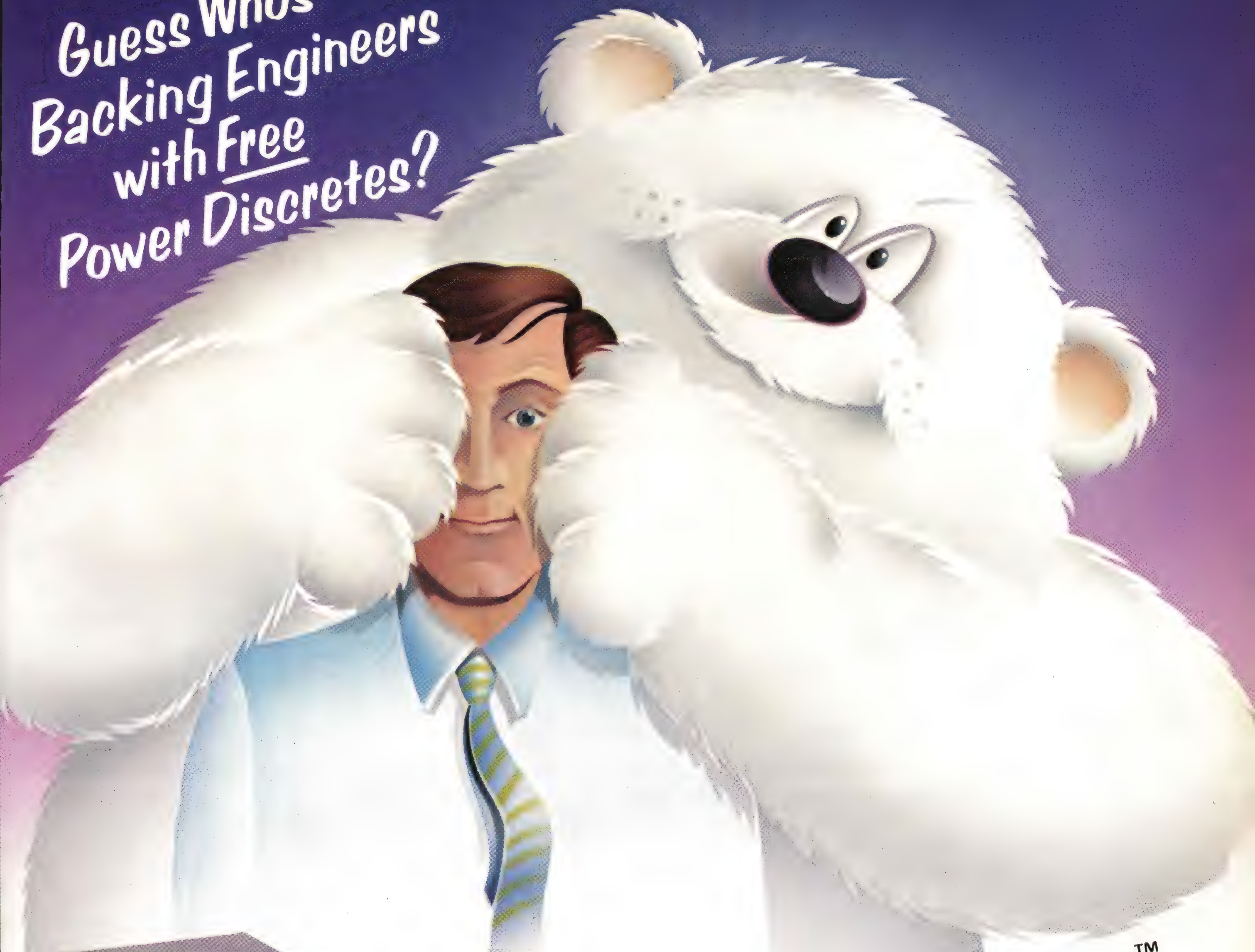

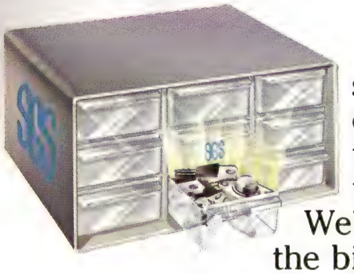

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CIRCLE NO 135

4 μPs AND μP-LIKE CHIPS *(continued)*

μP BUS COMPAT-IBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: ROM	KEY SPECIFICATIONS: RAM	KEY SPECIFICATIONS: PORT BITS	KEY SPECIFICATIONS: TIMER BITS	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	INTEL	8096	12 MHz	8k x (8)	232 x (8)	40	4 x (16)	NMOS 48-PIN 68-PIN PLCC, PGA	$10 (10k) NOW	EXAMPLE OF NEW CROP OF 16-BIT CONTROLLER μCs HAS 8 LEVELS OF FAST INTERRUPT, 10 BIT A/D
GENERAL	TI	7000	5 MHz	0	128 x (8)	32	1 x (8) (5-BIT) PRESCALE	NMOS +5V 40-PIN	$5.50 NOW	ROMLESS 1-CHIP μC. BASIC TI 7000 MODEL
GENERAL	TI	7020	5 MHz	2k x (8)	128 x (8)	32	1 x (8) (5-BIT) PRESCALE	NMOS +5V 40-PIN	$5.50 (5k QTY) NOW	1-CHIP μC. SOFTWARE COM-PATIBLE WITH TI 7000 μC
GENERAL	TI	7742	5 MHz	4k x (8) EPROM	256 x (8)	32	2 x (16) (5-BIT) PRESCALE	NMOS +5V 40-PIN	$38.40 NOW	ON-CHIP EPROM, SERIAL PORT PLUS 3 TIMERS & 256 BYTES RAM
GENERAL	TI	70CP160	5 MHz	16k x (8)	128 x (8)	32	1 x (8) (5-BIT) PRESCALE	CMOS +5V 40-PIN	$80 NOW	PIGGYBACK VERSION OF TI CMOS 1-CHIP μC WITH UP TO 16k-BYTE EPROM
GENERAL	TI	320C10 320CM10	20 MHz (5 MHz) 20 MHz 20 MHz	0 (+EXT) 1536 x (16) (+3XT)	144 x (16) 144 x (16)	0 0	0 0	CMOS +5V 40-PIN CMOS +5V 40-PIN	$50 NOW NA NOW	16/32-BIT COMBINED HIGH-SPEED CONTROLLER % NUMBER CRUNCHER (COULD ALSO BE IN **TABLE 1D**)
GENERAL	TI	320C25 320CM25	32, 40 MHz 32, 40 MHz	0 (+EXT) 4k x (16) (+EXT)	544 x (16) (+EXT) 544 x (16) (+EXT)	SERIAL SERIAL	0 0	CMOS +5V 68-PIN CMOS +5V 68-PIN (PGAs)	$134 2H86 NA 2H86	SECOND-GENERATION 32010, HAS ENHANCED FEATURES BUT LARGER, MORE EXPEN-SIVE CHIP

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

TABLE 5—ANALOG INTERFACES

EMPLOY A VARIETY OF CONVERSION TECHNIQUES AND HARDWARE-SOFTWARE TRADEOFFS. WIDESPREAD ACTIVITY IN THIS AREA, WITH IMPRESSIVE PRO-GRESS ACHIEVING VERY LOW-COST VERSIONS OF WHAT WERE VERY EXPENSIVE FUNCTIONS. MUCH OF CURRENT PROGRESS DIRECTED TOWARDS GREATER SPEED AND RESOLUTION WHILE HOLDING COSTS DOWN. MANY EXAMPLES HAVE VERY EASY-TO-USE μP INTERFACES.

μP BUS COMPAT-IBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS: A/D BITS	KEY SPECIFICATIONS: CHAN-NELS	KEY SPECIFICATIONS: D/A BITS	KEY SPECIFICATIONS: CONVERSION TECHNIQUE	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	ANALOG DEVICES	AD 7549	1.5 nSEC	—	3	12	CURRENT OUTPUT	LC^{2}MOS ±15V 20-PIN	$16.95 NOW	DUAL DAC
GENERAL	ANALOG DEVICES	AD 7820	1.36 nSEC	8	1	—	HALF FLASH	LC^{2}MOS +5V 20-PIN	$9.95 NOW	ON-CHIP TRACK/HOLD
GENERAL	ANALOG DEVICES	AD 7575	5 nSEC (50-kHz SAMPLING)	8	1	—	SUCC APPROX	LC^{2}MOS +5V 18-PIN	$5.50 NOW	ON-CHIP TRACK/HOLD. 100-nSEC μP ACCESS TIME
GENERAL	ANALOG DEVICES	AD 7225	5 nSEC	—	4	8	VOLTAGE OUT	LC^{2}MOS SINGLE OR DUAL 24-PIN	$18.50 NOW	CMOS QUAD DAC, HAS SEPARATE REFERENCE INPUTS & DOUBLE-BUFFERED LATCHES
GENERAL	ANALOG DEVICES	AD 575	30 nSEC	10	2	—	SUCC APPROX	I^2L +5, −12V 14-PIN	$12.95 NOW	COMPLETE A/D FITS IN SMALL 14-PIN PACKAGE
GENERAL	ANALOG DEVICES	AS 9702	5 nSEC	—	3	4	VOLTAGE OUT	BIPOLAR −5.25 & +5V 24-PIN	$48 NOW	TRIPLE 4-BIT PROVIDES UPDATE RATE OF 125 MHz & REDUCED COST OVER 3-CHIP ALTERNATIVE
GENERAL (8+4 OR 12 BIT DATA)	ANALOG DEVICES	AD 7572	5 nSEC 12.5 nSEC	12	1	—	SUCC APPROX	CMOS +5, −15V 28-PIN LCC	$47 $35 NOW	ON-CHIP REFERENCE & TRACK/HOLD
GENERAL	ANALOG DEVICES	IS 74	40,800 TO 630 RPM	10–16	1	—	TYPE-2 SERVO TRACKING LOOP	HYBRID ±12V 40-PIN	$279 NOW	RESOLVER-TO-DIGITAL CONVER-SION, ELIMINATES MECHANICAL TACH GEN PROGRAMMABLE RESOLUTION
GENERAL	OKI	M5204	600 nSEC	8	1	—	SUCCESS APPROX	CMOS +5V 18-PIN	$4.10 NOW	HAS ±1 LSB ACCURACY, TRACK/HOLD
GENERAL	OKI	M6253	100 nSEC	8	4	—	SUCC APPROX LADDER	CMOS +5V 18-PIN	$5.75 NOW	±½ LSB, BUILT-IN μP INTERFACE
GENERAL	OKI	M6219	40 nSEC	6	1	—	FLASH	CMOS +5V 18-PIN	$15 NOW	±1/S LSB, 11 MHz. TRACK/HOLD
GENERAL	MICRO NETWORKS	MN 5245	900 nSEC	12	1	—	SUBRANGING 7-BIT FLASH	HYBRID 40-PIN	$270 NOW	1-MHz THROUGHPUT RATE
GENERAL	MICRO NETWORKS	MN 7150-16 7150-8	50-kHz THRU-PUT	12	16, 8	—	SUCC APPROX	HYBRID 62-PIN	$248 NOW	COMPLETE DATA-ACQUISITION SYSTEM. INCLUDES MUXs, PGA, TRACK/HOLD

5 ANALOG INTERFACES *(continued)*

µP BUS COMPAT-IBILITY	SUPPLIER	MODEL	SPEED	KEY SPECIFICATIONS A/D BITS	CHAN-NELS	D/A BITS	CONVERSION TECHNIQUE	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	MICRO NETWORKS	MN 5284	50 µSEC	16	1	—	SUCC APPROX	HYBRID 32-PIN	$249 NOW	LOW POWER, SMALL SIZE
GENERAL	MICRO NETWORKS	MN 574A	35 µSEC	12	1	—	SUCC APPROX	HYBRID 28-PIN	$34.50 NOW	COMPLETE µP INTERFACE
GENERAL	MICRO NETWORKS	MN 6227	33-kHz THRU-PUT	12	1	—	SUCC APPROX	HYBRID 28-PIN	$69 NOW	TRACK/HOLD INCLUDED. TESTED DYNAMICALLY USING FFTs. 574A COMPATIBLE
GENERAL	MICRO NETWORKS	MN 5420	320 kHz	12	1	—	SUB-RANGING, AUTO-RANGING	HYBRID (MOD-ULE 3 x 4 x 5/8 IN.)	$1295 NOW	20-BIT DYNAMIC RANGE, FLOATING-POINT A/D. WITH HARDWARE AUTO-RANGING
GENERAL	MICRO NETWORKS	MN 5290	35 µSEC	16	1	—	SUCC APPROX	HYBRID 32-PIN	$175 NOW	EXTENDED TEMPERATURE, HIGH-RESOLUTION
GENERAL	MICRO NETWORKS	MN 565A	250 nSEC	—	1	12	CURRENT-STEERING SWITCHES	BIPOLAR ±12V 24-PIN	$16 NOW	HIGH-SPEED, SINGLE-CHIP, GUAR-ANTEED MONOTICITY
GENERAL	PMI	PM 7524	250 nSEC	—	1	8	R-2R LADDER	CMOS +5/+15V 16-PIN	$4.05 NOW	MULTIPLYING, WITH INPUT LATCHES
GENERAL	PMI	PM 7528	200 nSEC	—	2	8	R-2R LADDER	CMOS +5/+15V 20-PIN	$5.35 NOW	2 MULTIPLYING DACs MATCHED TO 1%
GENERAL	PMI	PM 7541 7545 7645	1 µSEC	—	1	12	R-2R LADDER	CMOS +5/+15V 18-PIN 20-PIN	$7.16 $7.20 NOW	4 QUADRANT MULTIPLY. 7541 IS SIM-ILAR TO AD 7521/41. 7545/7645 HAVE INPUT LATCHES
GENERAL	PMI	PM 8408	250 nSEC	—	4	8	R-2R LADDER	CMOS +5V 28-PIN	$8.03 NOW	4 DACs ON CHIP, MATCHED TO 1% & EACH WITH OWN REFERENCE INPUT
GENERAL	PMI	PM 8212	2 µSEC	—	2	12	R-2R LADDER	CMOS 24-PIN	$15.26 NOW	2 DACs ON CHIP

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

TABLE 6—CONSUMER AND ENTERTAINMENT DEVICES

PARTS DEVELOPED FOR HIGH-VOLUME TV-GAME AND HOME-COMPUTER MARKETS. HAVE SUFFICIENT GENERALITY TO ALSO BE USED ELSEWHERE. ACTIVITY HAS BEEN REDUCED BECAUSE OF SLUMP IN ELECTRONIC-GAME MARKET. HOWEVER, CURRENT WORLDWIDE ACTIVITY IN DEVELOPING DIGITAL AUDIO, µP-CONTROLLED VCRs AND DIGITAL TV SHOULD PRODUCE MORE FALL-OUT CIRCUITS FOR THIS TABLE IN THE FUTURE.

µP BUS COMPAT-IBILITY	SUPPLIER	PART NO	SPEED	OTHER FEATURES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL (SERIAL 3-WIRE)	NATIONAL	DS 8906	120 MHz	REFERENCE OSCILLATOR, PHASE COMPARATOR, CHARGE PUMP, DUAL MODULUS PROGRAMMABLE DIVIDER, & 20-BIT SHIFT REG FOR SERIAL DATA ENTRY	BIPOLAR ECL/I²L 20-PIN	$7.60 NOW	AM/FM DIGITAL PLL FREQUENCY SYNTHESIZER PROGRAMMABLE FROM µP VIA SERIAL INPUT
GENERAL (SERIAL 3-2 WIRE)	NATIONAL	DS 8908	120 MHz	REFERENCE OSCILLATOR, PHASE COMPARATOR, CHARGE PUMP, DUAL MODULUS PROGRAMMABLE DIVIDER, & 19-BIT SHIFT REG FOR SERIAL DATA ENTRY	BIPOLAR ECL/I²L 20-PIN	$8.20 NOW	AM/FM DIGITAL PLL FREQUENCY SYNTHESIZER PROGRAMMABLE FROM µP VIA SERIAL PORT
GENERAL (SERIAL 3-WIRE)	NATIONAL	DS 8910	120 MHz	REFERENCE OSCILLATOR, PHASE COMPARATOR, CHARGE PUMP, DUAL MODULUS PROGRAMMABLE DIVIDER, & 19-BIT SHIFT REG FOR SERIAL DATA ENTRY	BIPOLAR ECL/I²L 20-PIN	$7.40 NOW	AM-ONLY DIGITAL PLL FREQUENCY SYNTHESIZER PROGRAMMABLE FROM µP VIA SERIAL PORT
GENERAL	NATIONAL	DS 8911	225 MHz	DIGITAL PLL FOR USE AS LOCAL OSCILLATOR. UP CONVERSION TUN-ING. ONBOARD PROGRAMMABLE MIXER WITH HIGH DYNAMIC RANGE. (LOW 0.5-mA STANDBY CURRENT)	"BIPOLAR CMOS" 24-PIN SMALL OUT-LINE 28-PIN PCC	$10.25 NOW	AM/FM/TV SOUND UP CONVERSION FREQUENCY SYNTHESIZER
GENERAL (SERIAL 2-WIRE)	SIEMENS	TBA 130	100 kHz	FM-IF AMPLIFIER, BUS CONTROL I²C, & SCART INTERFACES	BIPOLAR 18-PIN	$2.08 NOW	RADIO & TV USE
GENERAL (SERIAL)	SIEMENS	SDA 3202	1.36 GHz	PLL FREQUENCY SYNTHESIZER	BIPOLAR 18-PIN	$3.59 NOW	SERIAL INPUT
GENERAL (SERIAL 3-WIRE)	SIEMENS	SDA 3112	32 MHz	PLL FREQUENCY SYNTHESIZER (2 GHz WITH AVAILABLE PRESCALER)	BIPOLAR 18-PIN	$3.20 NOW	FOR CATV
GENERAL (SERIAL 3-WIRE)	SIEMENS	SDA 3203	1.36 GHz	PLL FREQUENCY SYNTHESIZER	BIPOLAR 22-PIN	$3.59 NOW	
GENERAL (SERIAL 3-WIRE)	SIEMENS	SDA 2120	120 MHz	PLL FOR AM/FM RECEIVERS	BIPOLAR 22-PIN	$4.78 NOW	
GENERAL (SERIAL 3-WIRE)	SIEMENS	SDA 2131	500 kHz	DRIVES 16 LEDs WITH 10 mA	BIPOLAR 20-PIN	$1.60 NOW	DISPLAY DRIVER

Continued on pg 165


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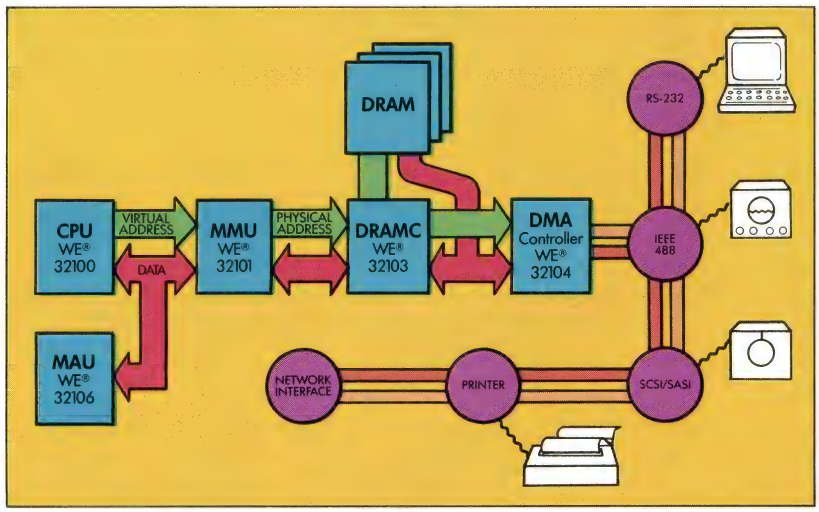

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The Dynamic RAM Controller (DRAMC) can be programmed to optimize your memory speed to the system.

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We've developed today's most highly-optimized C language compiler, ensuring compact, high-performance code without manual optimization. Also available: compilers for high-level languages such as FORTRAN, COBOL, Pascal and BASIC. To keep you on the leading edge, the AT&T microsystem will continue to evolve with the UNIX System V standard.

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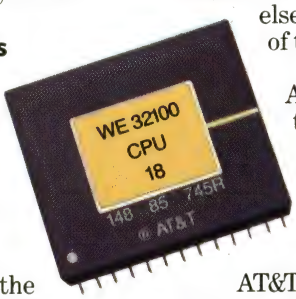

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CIRCLE NO 136

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6 CONSUMER AND ENTERTAINMENT DEVICES *(continued)*

µP BUS COMPATIBILITY	SUPPLIER	PART NO	SPEED	OTHER FEATURES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL (SERIAL 2-WIRE)	SIEMENS	TDA 6200	100 kHz	HOST µP CAN CONTROL BALANCE, BASE & TREBLE	BIPOLAR 28-PIN	$5.75 NOW	STEREO SOUND CONTROL
GENERAL	SIGNETICS	NE 5050	100k BPS (LESS ON POWER LINE)	RECEIVER/TRANSMITTER FOR SENDING DATA OVER TWISTED PAIRS OR 60-Hz POWER LINES. USES CARRIER ON/OFF MODULATION & CAN DO CARRIER SENSE MULTIPLE ACCESS/COLLISION DETECTION (CSMA/CD).	BIPOLAR +12V 20-PIN	$1.95 NOW	LOW-PERFORMANCE BUT LOW-COST BUILDING BLOCK FOR HOME LANs (FOR SECURITY CONTROL OR DATA TRANSFER)

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

TABLE GROUP 7—TELECOMMUNICATION DEVICES

7A ANALOG TELECOMMUNICATION DEVICES

FOR EXISTING ANALOG PORTIONS OF INTERNATIONAL TELEPHONE NETWORK. INCLUDES MODEMS, CODECS, ETC. NOTE THAT SOME ENTRIES ARE FOR ASSOCIATED COMPONENTS THAT MAY NOT DIRECTLY INTERFACE TO µPs.

µP BUS COMPATIBILITY	SUPPLIER	PART NO	SPEED	OTHER FEATURES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	SMC	COM 9046	3.58 MHz	SPEECH SCRAMBLER, DESCRAMBLER	NMOS +5V 14-PIN	$4.75 NOW	FULL DUPLEX, LOW POWER. FOR PORTABLE EQUIPMENT
GENERAL	OKI	M 6927 6947	1200 BAUD	FSK, HALF-DUPLEX CCITT V-23 BELL 202	CMOS 28-PIN	$8 NOW	MODEMS
GENERAL	OKI	M 6932 6933		CODEC & PCM FILTER µ-LAW A-LAW	CMOS 16-PIN	$8.10 NOW	VARIABLE SAMPLING RATE FOR 6932 & FIXED INTERVAL FOR 6933
GENERAL	OKI	M 6914		16 x 4 x 3 BITS	CMOS 120-PIN	$90 NA	SWITCH MATRIX WITH 4 INPUT LINES, 4 OUTPUT LINES & PARITY CHECK
GENERAL	NATIONAL	MM 74HC943	300 BAUD	BELL-103 COMPATIBLE. ON-CHIP HYBRID & LINE DRIVER. 3.579-MHz CRYSTAL	CMOS +5V 20-PIN	$7.95 NOW	FSK MODEM, INDUSTRY STANDARD
GENERAL	NATIONAL	TP 3051 3056	2.048 MHz	PARALLEL DATA I/O, µ-LAW COMPANDING, LOW NOISE. PARALLEL DATA I/O, A-LAW COMPANDING, LOW NOISE	CMOS ±5V 20-PIN 20-PIN PCC	$10.30 NOW	CODEC/FILTER COMBO FOR USE WITH TP3120 LINE-CARD CONTROLLER OR DIRECT µP INTERFACE
GENERAL	NATIONAL	TP 3058 3059	2.048 MHz	PARALLEL DATA I/O, µ-LAW COMPANDING, LOW NOISE. PARALLEL DATA I/O, A-LAW COMPANDING, LOW NOISE	CMOS ±5V 22-PIN 28-PIN PCC	NA 3Q86	SIMILAR TO 3051 & 3056 BUT WITH IMPROVED µP INTERFACE
GENERAL	NATIONAL	TP 3070	4.096 MHz	SERIAL DATA I/O, A-LAW/µ-LAW PROGRAMMABLE. ALSO PROGRAMMABLE: GAIN, HYBRID BALANCE, SLIC LATCHES, TIME-SLOT ASSIGNMENT	CMOS 20-PIN 20-PIN PCC	NA 4Q86	CODEC/FILTER COMBO. SERIAL & PARALLEL VERSIONS TO BE AVAILABLE
GENERAL	NATIONAL	TP 3110/12/ 20/21	2.048 MHz	32 CHANNELS VOICE/DATA, HDLC CONTROL SECURITY, 2 OR 4 SERIAL TIME-DIV-MULTIPLEXED PORTS	NMOS +5V 40-PIN 44-PIN PCC	$17.50 NOW	TIME-DIV-MULTIPLEXED SWITCH. FOR USE WITH TP3051/56 COMBOS OR UART
GENERAL	NATIONAL	TP 3155	2.048 MHz	UP TO 8 CHANNELS	CMOS +5V 20-PIN 20-PIN PCC	$5.40 NOW	TIME-SLOT ASSIGNER
GENERAL	NATIONAL	TP 3202 3204	—	MAGNETIC COMPENSATION, −48V OR +5V RELAY DRIVERS. ALSO RING, TRIP, OFF-HOOK DETECTION	BIPOLAR ±5V 20-PIN 20-PIN PCC	$5.40 NOW	SLIC. REDUCES SIZE & COST OF ISOLATION TRANSFORMER
GENERAL	NATIONAL	TP 3330	1200 BAUD	BELL 212A V.22, FULL DUPLEX, USART ON BOARD, AUTO ANSWER, DTMF DIALER	CMOS 28-PIN	NA 4Q86	MODEM
GENERAL	AMD	AM 7910 7911	300, 600, 1200 BPS, SELECTABLE	FSK, COMPATIBLE WITH BELL 103, 113, 108 & BELL 202; CCITT V.21, V.23 SWITCHED NETWORKS. RS232/CCITT V.24	NMOS ±5V 28-PIN	$24.55 NOW	SINGLE-CHIP MODEM. DSP. NO EXTERNAL FILTERS REQUIRED
GENERAL (SERIAL OR PARALLEL DATA INTERFACE)	AMD	AM 79C12 AM 79C14	300, 1200 BPS 1200, 2400 BPS	NO EXTERNAL FILTERS REQUIRED. DTMF PROGRESS TONES DETECTION 4-2 WIRE HYBRID. UART. HANDSHAKE PROTOCOL. DSP TECHNOL. 79C12 IS DQPSK/FSK & 79C14 IS QAM/DQPSK	CMOS +5V 40-PIN 44-PIN PLCC	$48 (EST) 2Q86 NA 4Q86	SINGLE-CHIP MODEM

7A ANALOG TELECOMMUNICATION DEVICES *(continued)*

µP BUS COMPAT-IBILITY	SUPPLIER	PART NO	SPEED	OTHER FEATURES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL (SERIAL)	AMD	AM 7901ADC 7901BDC 7905ADC	4.096 MHz (PCM)	USER-PROGRAMMABLE DIGITAL FILTERS. DYNAMIC TIME-SLOT ASSIGNMENT. CONTROL INTER-FACE TO 7950/51 SLIC	NMOS 28-PIN 24-PIN	$19.70 NOW	CODECS, USING DSP TECHNIQUES. A-LAW, µ-LAW & 16-BIT LINEAR OPTIONS
GENERAL	AMD	AM 7950 7953	4.096 MHz	PROGRAMMABLE IMPEDANCE, LOOP DETECT THRESHOLD, WITH ON-CHIP SWITCHING REG	BIPOLAR (HI V)	$19.70 NOW	PROGRAMMABLE LINEAR LINE FEED & PROGRAMMABLE CONSTANT-CURRENT LINE FEED

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

7B DIGITAL TELECOMMUNICATION DEVICES

FOR DIGITAL PORTIONS OF THE INTERNATIONAL TELEPHONE NETWORK. THE ALL-DIGITAL ISDN (INTEGRATED SERVICES DIGITAL NETWORK) IS JUST BEGINNING TO SEE TRIALS; HOWEVER SOME OF THESE DEVICES HAVE ALREADY BEEN DESIGNED INTO PBXs.

µP BUS COMPAT-IBILITY	SUPPLIER	PART NO	SPEED	OTHER FEATURES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	MOTOROLA	MC 145422/ 5426	80k BPS FULL DUPLEX	UNIVERSAL DIGITAL LOOP TRANS-CEIVER (UDLT) MASTER/SLAVE	CMOS 22-PIN	$11 (25k QTY) NOW	ISDN-COMPATIBLE, ONE 26-AWG WIRE PAIR UP TO 2-km SIMUL-TANEOUS VOICE AND DATA TRANSMISSION
GENERAL	MOTOROLA	MC 145418/ 5419	80k BPS FULL DUPLEX	DIGITAL LOOP TRANSCEIVER (DLT) MASTER/SLAVE	CMOS 22-PIN	$7.50 (25k QTY) NOW	ISDN COMPATIBLE, LOW-COST VER-SION OF UDLT
GENERAL (8-BIT PARALLEL)	ROCKWELL	8040 8050 8060	T-1 SPECS	FAMILY MEETS BELL T-1 STD AND IS COMPATIBLE WITH DEC-NORTHERN TELECOM COMPUTER TO PBX INTERFACE. MUX/DEMUX 24 CHANNELS OVER PAIR OF LOW-COST SERIAL WIRES	NMOS +5V 40-PIN 28-PIN 28-PIN	$18.35 $7.40 $17.95 NOW	8040 IS TIME-SLOT INTERCHANGE MEMORY, 8050 IS SERIAL TRANSMIT-TER, AND 8060 IS SERIAL RECEIVER
SERIAL OR GENERAL (8-BIT)	ROCKWELL	8070	T-1 (1.544 MHz) ½ T-1C (0.576 MHz) CEPT (2.048 MHz)	TRANSCEIVER DEVICE MEETS BELL T-1 STD, EXTENDED FRAM-ING, CLEAR CHANNEL SERIAL EUROPEAN PCM-30. COMPATIBLE WITH ATT DMI PROTOCOL AS WELL AS NORTHERN TELECOM CPI PROTOCOL	CMOS +5V 64-PIN QUIP 68-PIN J-LEAD	$26 NOW	ONBOARD B8ZS, HD83 ENCOD-ING/DECODING. ONBOARD CRC GENERATION & DETECTION. SUITED TO CHANNEL BANK APPLICATIONS. PROVISIONS FOR SUPPORT OF SIC-96
GENERAL	AMD	79C30	192k BPS	CCITT ISDN COMPATIBLE	CMOS 40-PIN	$49.75 1Q86	DIGITAL SUBSCRIBER CONTROLLER (DSC) FOR VOICE/DATA TERMINAL
GENERAL	AMD	79C31	192k BPS	CCITT ISDN COMPATIBLE	CMOS 28-PIN	$20.75 3Q86	DIGITAL EXCHANGE CONTROLLER (DEC) FOR SIMPLE, INTELLIGENT NETWORK TERMINALS & PABX LINE CARDS
GENERAL	AMD	79C32	192k BPS	CCITT ISDN COMPATIBLE	CMOS 40-PIN	$24 1Q86	ISDN DATA CONTROLLER (IDC) SUPPORTS ACCESS FOR DATA TERMINALS
GENERAL	AMD	79C33	160k BPS	SUPPORTS 2B+D DATA TRANSFER PER CCITT ISDN	CMOS 24-PIN	NA 3Q86	TRANSCEIVER ECHO CANCELLER (TEC) PROVIDES A CENTRAL OFFICE AND 2-WIRE PABX SOLUTION
GENERAL	AMD	79C36	—	CCITT ISDN COMPATIBLE	BIPOLAR 18-PIN	$11.75 1Q86	SUBSCRIBER POWER CONTROLLER FOR REGULATING DC VOLTAGES
GENERAL	AMD	79C38	—	CCITT ISDN COMPATIBLE	BIPOLAR 22-PIN	$20 2Q86	QUAD EXCHANGE POWER CON-TROLLER (QEPC) FOR REGULATING 40V TO FOUR LINES IN PABX, TERMI-NALS AND CENTRAL OFFICES
GENERAL	AMD	7970	5 MHz	CCITT GROUP 3 AND GROUP 4 FAX-COMPATIBLE DOCUMENT IMAGE COMPRESSION/EXPANSION PROCESSOR	NMOS 68-PIN	$240 NOW	DUAL-BUS, ON-CHIP DMA, FULL-DUPLEX OPERATION. (ALSO IN **TABLE 1D**)
GENERAL (8-BIT)	SIEMENS	2070	4 MHz 512k BPS	CONTROLS FOR TWO 64k-BPS ISDN B CHANNELS & ONE ISDN 16k-BPS D CHANNEL	CMOS 24-PIN	$15 NOW	ISDN LAYER-2 FUNCTION FOR S 4-WIRE BUS. SOFTWARE CONTROL
GENERAL	SIEMENS	2080	192k BPS	4-WIRE ISDN S BUS INTERFACE, CCITT 1.431	CMOS 22-PIN	$15 NOW	ISDN LAYER-1 FUNCTION FOR S 4-WIRE BUS. HARDWARE INTERFACE
GENERAL (8-BIT)	SIEMENS	82520	4-MHz DATA RATE	TWO INDEPENDENT FULL-DUPLEX HDLC CHANNELS. X.25 LAPB/LAPD PROTOCOL. FIFO BUFFER	CMOS 28-PIN	$23 NOW	GENERAL-PURPOSE DATA-LINK CON-TROLLER FOR ASYNCHRONOUS AND SYNCHRONOUS USE
GENERAL	SIEMENS	2085	512k BPS	COMPLETE ISDN S BUS ON 1 CHIP. COMBINES 2070 & 2080	CMOS 40-PIN	NA 3Q86	ISDN SUBSCRIBER ACCESS CON-TROLLER. 1 CHIP
GENERAL	SIEMENS	2090	2 x 160k BPS (2 x 144k BPS FOR USER DATA)	ISDN U 2-WIRE SUBSCRIBER LOOP INTERFACE. WOULD GO AT EACH END OF EXISTING LOOPS. CAPABLE OF HANDLING LONGER DISTANCES (OVER 3 MI)	CMOS NA	NA 3Q87	ADAPTIVE ECHO-CANCELLING APPROACH. SOPHISTICATED LARGE CHIP, SO WILL BE EXPENSIVE. 2095 IS LOWER ALTERNATIVE FOR SHORTER, SIMPLER SUBSCRIBER LOOPS

7B DIGITAL TELECOMMUNICATION DEVICES *(continued)*

µP BUS COMPAT-IBILITY	SUPPLIER	PART NO	SPEED	OTHER FEATURES	TECHNOLOGY PACKAGE	PRICE (100) AVAIL	COMMENTS
GENERAL	SIEMENS	2095	2 x 160k BPS (2 x 144k BPS FOR USER DATA)	ISDN U 2-WIRE SUBSCRIBER LOOP INTERFACE. WOULD GO AT EACH END OF EXISTING LOOPS. RESTRICTED TO SHORTER DISTANCES (UNDER 2 MI)	CMOS 18-PIN	$15 4Q86	BURST MODE OR PING-PONG APPROACH. LOWER COST THAN 2090, BUT LIMITED TO SHORTER SUBSCRIBER LOOPS
GENERAL	MITEL	8952	NA	FRAMES & FORMATS DATA PACKETS ACCORDING TO X.25 (LEVEL 2) OF CCITT	CMOS +5V 28-PIN	$11.25	HDLC PROTOCOL CONTROLLER (COULD ALSO BE IN **TABLE 1B**). PROVIDES XX CHANNEL REQUIRED BY MITEL DNIC
6800 ST-BUS	MITEL	8975	2048k BPS (1544k T1 LINK)	FOR USE BETWEEN SERIAL 2048k-BPS MITEL ST-BUS & BIDIRECTIONAL 1544k-BPS T1 TRUNK	CMOS +5V 20-PIN 24-PIN LCC	$35 NOW	DIGITAL TRUNK INTERFACE CIRCUIT
6800 ST-BUS	MITEL	8978	2048k BPS	FOR USE BETWEEN SERIAL 2048k-BPS MITEL ST-BUS & BIDIRECTIONAL 2048k-BPS CEPT/CCITT TRUNK	CMOS 20-PIN 28-PIN LCC	$40 NOW	DIGITAL TRUNK INTERFACE CIRCUIT
6800 ST-BUS	MITEL	8970 DLIC	256k BPS	4-WIRE INTERFACE SIMILAR TO ISDN S, USING AMI LINE CODE	CMOS 40-PIN	$23.50 NOW	DIGITAL LINE INTERFACE CIRCUIT (DLIC). WAS DESIGNED BEFORE ISDN
6800 ST-BUS	MITEL	8972 DNIC	80k, 160k BPS	2-WIRE ISDN U INTERFACE	CMOS 22-PIN	$37 NOW	DIGITAL NETWORK INTERFACE (DNIC). USES ECHO CANCELLATION
6800	MITEL	8930 SNIC	192k BPS (144k BPS FOR USER DATA)	ISDN 4-WIRE S INTERFACE	CMOS NA	NA 3Q86	S-BUS INTERFACE (SNIC). UNLIKE EARLIER 8970
6800	MITEL	8980 8981	2048k BPS	256 x 256 CROSSPOINT SWITCH 8-LINE x 32 CHANNEL IN/OUT 128 x 128 CROSSPOINT SWITCH 4-LINE x 32 CHANNEL IN/OUT	CMOS 40-PIN CMOS 40-PIN	$29.50 NOW $10.85 NOW	DIGITAL CROSSPOINT SWITCH
GENERAL	NATIONAL	TP 3400	144k BPS	TWO B + ONE D CHANNEL, UP TO 6k-FT BURST MODE TCM	CMOS 20-PIN	NA 3Q86	PRE-ISDN DIGITAL LOOP TRANSCEIVER
8051 80186	INTEL	29C53	ISDN STD	4-WIRE ISDN S LOOP INTERFACE	CMOS NA	NA 1H86	ISDN DIGITAL LINE EXCHANGE CONTROLLER
8051 80186	INTEL	29C55	160k BPS	ISDN 2-WIRE U INTERFACE WITH ECHO CANCELLING. (2B+D) CHANNELS	CMOS NA	NA 1H86	DIGITAL COMMUNICATIONS INTERFACE TRANSCEIVER/CONTROLLER

NA = NOT AVAILABLE
— = NOT APPLICABLE
SPACE LIMITATIONS PREVENT INCLUSION OF ALL AVAILABLE DEVICES. CONTACT MANUFACTURERS FOR MORE INFORMATION.

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CIRCLE NO 139

Custom microcontroller cell reduces required logic in µP systems

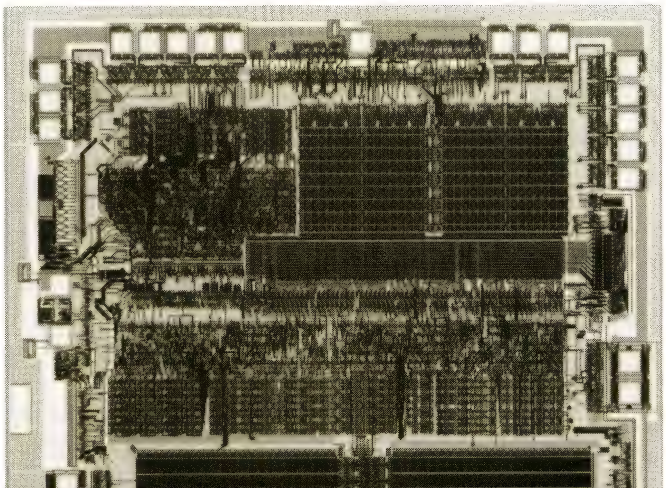
By using a custom microcontroller cell instead of a multiplexed standard part in your system design, you can reduce your design's chip count, expand control memory, and enhance system performance. The UC51 microcontroller cell, a functional equivalent of the standard 80C51, gives you access to 103 functional signals.

Matt Townsend, *Intel Corp*

When you design a microcontroller system around a standard microcontroller chip, you may not be able to connect system circuitry to many of the logic-signal lines, because the signals are multiplexed. Unless you add logic, you can't use all the signals. However, if you base your system on a custom implementation of a microcontroller instead of on a standard part, you'll have access to all the cell's signal lines. To design such a custom IC, you start with a microcontroller cell and work with the manufacturer to design the rest of the circuitry. The resulting system will have less logic, more program memory, and better performance than one built around a packaged microcontroller.

The 80C51 microcontroller IC from Intel illustrates the problem that standard µPs pose for the designer. The 80C51 has 61 signal lines: four 8-bit I/O ports, 16 address lines, and 13 control signals. The manufacturer puts the chip in a 40-pin package by multiplexing two of the ports with the address lines and a third port with eight control signals (**Fig 1**).

Because some of the signal lines on the 80C51 are multiplexed, you have to give up some of the chip's functions to implement others. For example, in applications using external memory, you can't use port 0. And depending on how you access the memory, you may not



Functionally equivalent to the 80C51 IC, *the UC51 cell (shown here integrated with I/O circuitry) makes available all of the signals that are multiplexed on the 80C51. The UC51 can address as much as 16k bytes of program ROM. You can put standard cells on chip with the UC51 to create a custom processor IC.*

Because some of the signal lines on the 80C51 are multiplexed, you have to give up some of the chip's functions to implement others.

be able to use port 2. What's more, two of the signals that share pins with port 3 are necessary for implementing the external memory, so either you can't use those two pins for port 3 or you have to add logic so you can use both port 3 and the signals.

In applications using on-chip peripherals such as the serial UART port, your design must control the peripherals through pins that are assigned to port 3. On-chip peripherals, therefore, also limit access to port 3.

Of course, one way to gain access to the 80C51's I/O ports would be to attach an I/O-expansion peripheral chip—such as the manufacturer's 8255 programmable peripheral-interface IC—directly to the microcontroller's processor bus, which is available through ports 0

Simulating and testing your UC51-based IC

To help customers verify the custom ICs they design around the UC51 microcontroller cell, Intel supplies both a behavioral cell model and design tools that help you debug your design.

A behavioral model of a cell describes the cell's behavior as observed at its inputs and outputs. Such a model is much less complex than a structural model, which describes the components of a cell. A structural model for the UC51, for example, would include as many as 6000 gates, not including modeling for on-chip RAM and ROM.

A behavioral model is actually a software subroutine that behaves in a simulation the same way that a cell would behave in a circuit. Behavioral models take up less space in memory and respond more quickly to a simulator's request for information than do structural models. This increase in response time can be as great as several orders of magnitude, depending on the complexity of the cell. In the case of a UC51 cell, the simulator need only simulate the random logic in conjunction with the UC51 subroutine. In contrast, a simulator using a structural model of such a complex cell would have to simulate the random logic in conjunction with 6000 gates.

Because a behavioral model functions in a simulator the same way that a structural model does, however, you can use it with structural models in a simulator. For example, a simulator for your custom UC51-based chip could include both the behavioral model of the UC51 and structural models of the applications logic in your design.

Besides providing a behavioral model of the UC51, the company offers a design system that helps you debug and verify your custom-IC design. The design system lets you use emulator-like commands to set values in internal registers and flags. Using the commands, you can introduce special circuit conditions to verify logic. (These special conditions might be hard to obtain if you had to use only input signals for access to logic.) You can also observe the values of internal signals, including registers and flags. For debugging program operations, you can use trace and breakpoint features like those found in an emulator. The design software also includes design checks that detect problems such as pulse-width and set-up-and-hold violations.

When you've debugged your design, you can create a test program for your UC51-based design with the help of a hardware test facility. The test facility, which consists of a ring of test logic and buffers around the UC51, isolates the cell from surrounding circuitry. By isolating the microcontroller, you can apply test patterns that are similar to ones that you'd apply to the 80C51. In fact, your test program can include test programs originally written for the 80C51. The company supplies you with test patterns for the UC51 cell; the only patterns you have to write are patterns for testing your custom applications logic.

To develop the test programs for the applications logic you design around the UC51, you can use an extended version of the ASM51 assembler. Using assembly language statements, you describe the UC51 stimulus for your applications logic in a source-level assembly-language test program. The UC51 executes the program and stimulates your applications logic. The test program and a pattern of expected responses from your applications logic define the complete test for that logic. The company then translates your test program into code for its production test equipment.

and 2. The 8255 contains three 8-bit ports that connect to one 8-bit data-bus port. By connecting the data-bus port to the microcontroller bus, you would add three 8-bit ports to the system. Counting the microcontroller bus, your system would then have four ports, the number specified for the 80C51.

Adding an I/O-expansion chip won't help you minimize pc-board size, cost, and power consumption, however—the extra circuitry that you need to add includes not only the 40-pin 8255, but memory-address decoding and bus-demultiplexing ICs.

A better solution would be to design your system around the customizable cell version of the microcontroller, the UC51. Because the UC51 is a functional equivalent of the 80C51, you can use it to create the same basic type of design, but your new design will deliver better performance. Further, your new system will contain fewer ICs than would an 80C51 implementation. Because the UC51 doesn't include I/O multiplexing circuitry, it gives you access to all 103 signal lines from the chip's internal circuitry. Because you won't need to perform I/O expansion, your system design will include less logic.

Microcontroller cell offers all I/O signals

Because the UC51 cell doesn't contain all the I/O-multiplexing hardware found on the 80C51, you can connect other system circuitry to any ports and control-signal lines. Except for the data bus, none of the UC51's ports are bidirectional. The cell's I/O consists of four 8-bit input ports, four 8-bit output ports, an 8-bit bidirectional processor bus, the most significant 16 bits of the program-counter register, processor-bus-control pins, and on-chip-peripheral signals **(Fig 1b)**.

The UC51's expanded pinout lets you connect system circuitry to a number of signals that are unavailable on the 80C51. Pin 39 of the 80C51, for example, can operate as one of five signal lines: an input line, an output line, a bidirectional line, an address line A_0, or a data line D_0. On the UC51 cell, you can connect your circuit to any signal line. For bidirectional I/O, you can select an I/O element from the company's standard-cell library that combines port 0's separate input and output lines to form a bidirectional line.

Because most of its signals aren't multiplexed, the custom chip you design with the UC51 won't require as much logic as the 80C51 chip does. For example, the 80C51 application in **Fig 2a** requires 16 additional inputs and outputs; the logic that demultiplexes the I/O is equivalent to about 300 2-input gates. The custom

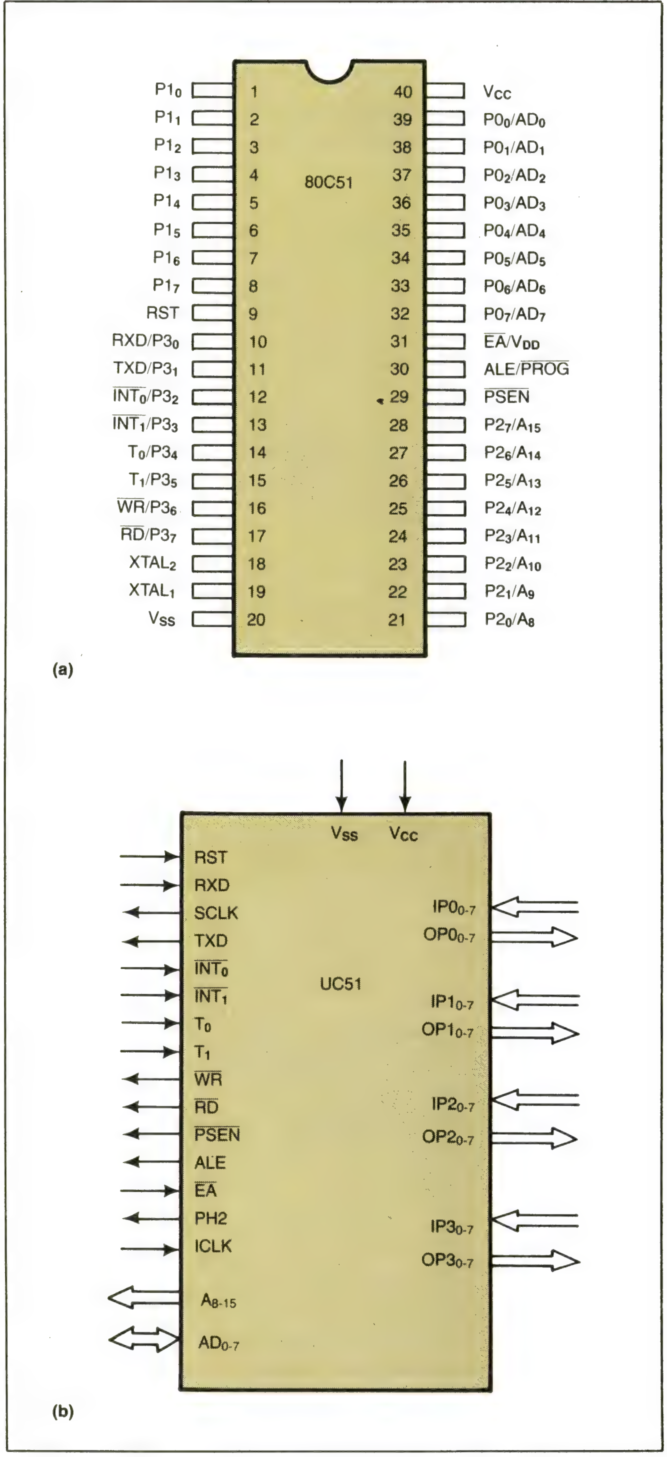


Fig 1—Because many of the control signals on the 80C51 microcontroller chip are multiplexed (a), *the designer must give up some of the chip's functions to implement others. The UC51 customizable cell version of the chip, however, doesn't have multiplexed signal lines* ***(b),*** *so you can use all of its functions at the same time.*

The UC51 cell doesn't contain all the I/O-multiplexing hardware found on the 80C51, so you can connect system circuitry to all ports and control signals.

UC51 implementation in **Fig 2b** doesn't require this support logic.

Although you could minimize the number of chips in an 80C51-based system by integrating the demultiplexing and applications logic onto a custom chip (such as a gate array or standard-cell IC), the resulting system might still prove to be expensive and inefficient compared to one based on the UC51 cell. For one thing, to connect circuitry to all of the cell's signals, the custom IC would have to have a high pin count. It would certainly need more than 40 pins, and it might even need more than 68 pins. Not only are components with high pin counts expensive, but they increase a pc board's wiring complexity.

Another design constraint of the 80C51 is that it has a fixed amount—4096 bytes—of on-chip ROM. For

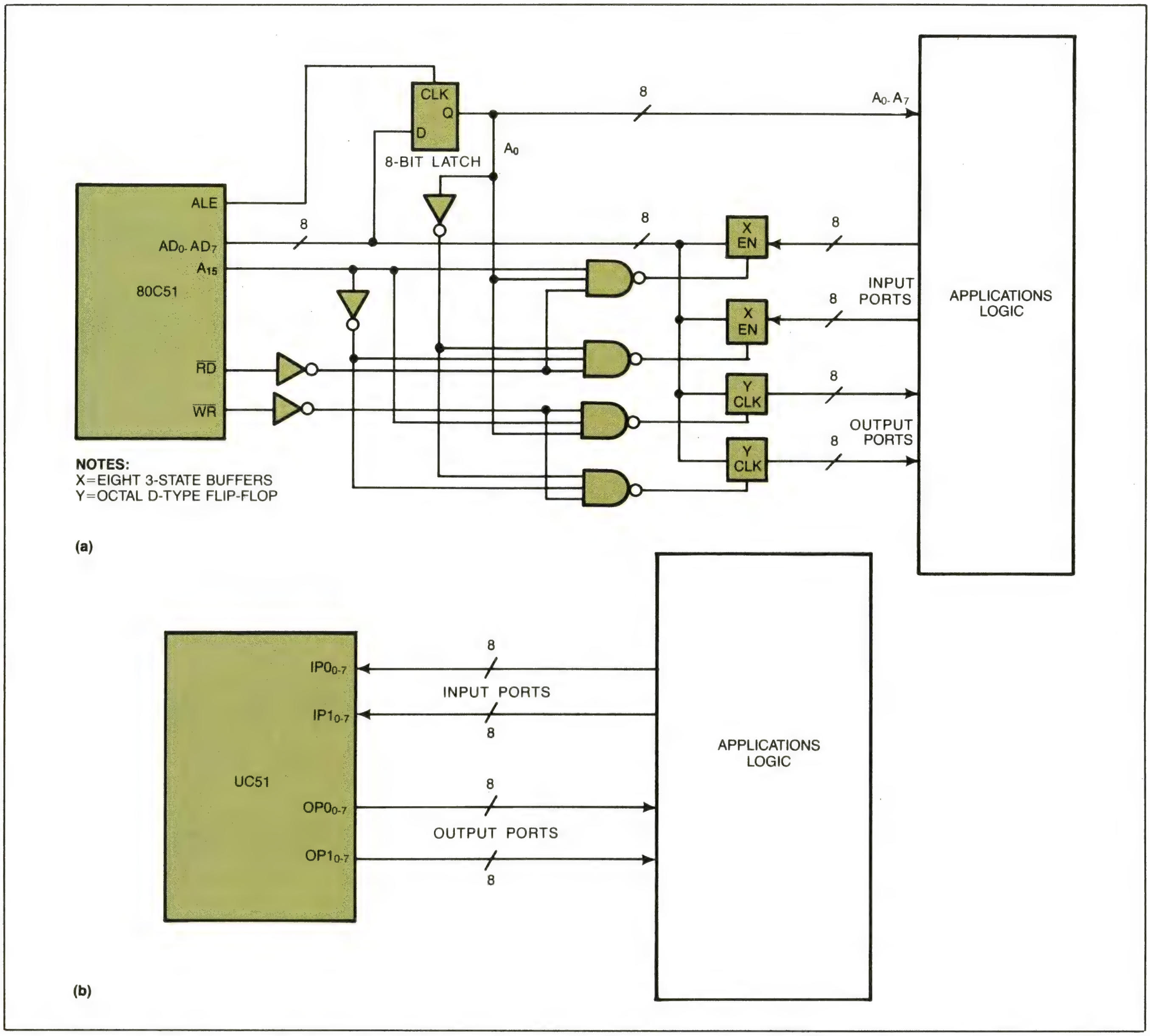


***Fig 2—Decoding logic creates two ports** in a typical 80C51 system design **(a)**. To add 16 inputs and outputs to the system, you need to add about 300 gates of logic. In a similar system implemented with the UC51 cell, you can connect four ports directly to the UC51 without I/O-expansion logic **(b)**.*

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applications that include a number of functions and on-chip peripherals, program code often takes up more than 4096 bytes of ROM. In such a case, you must put the additional code in external storage and use the microcontroller's data and address lines, through ports 0 and 2, to access the external storage.

If you base your design on a customized UC51, however, you can put as much memory as you need onto your custom chip, avoiding troublesome external storage. You can add as much as 16k bytes of ROM to the chip in 4k-byte steps. The UC51 comes in versions that can access any of the possible ROM sizes. Note, however, that external storage always requires I/O lines that you can't then use to control I/O devices. Even if you use the UC51, external program storage can require more pins in your IC design than all on-chip memory requires.

Putting 16k bytes of ROM on your custom chip may not seem economical when you consider the relatively low price of discrete ROM chips. However, including all necessary ROM on chip reduces pc-board size and parts count, thus lowering the board's power consumption and increasing its reliability. You also save the cost of programming additional ROMs for your system and keeping them in stock.

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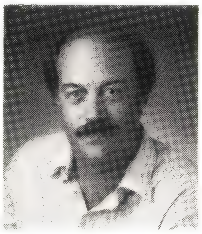
Author's biography



Matt Townsend is the Technical Marketing Manager at Intel's Custom Products Div in Chandler, AZ, where he serves as the technical interface between customers and the company's standard-cell and VLSiCEL product groups. Matt, who has been with the company for 14 years, was previously employed by Motorola, Quadri Corp, Dataproducts, and Ford Aerospace. He holds a BSEE from Arizona State University and has had two patents granted. His hobbies include horseback riding and building construction.

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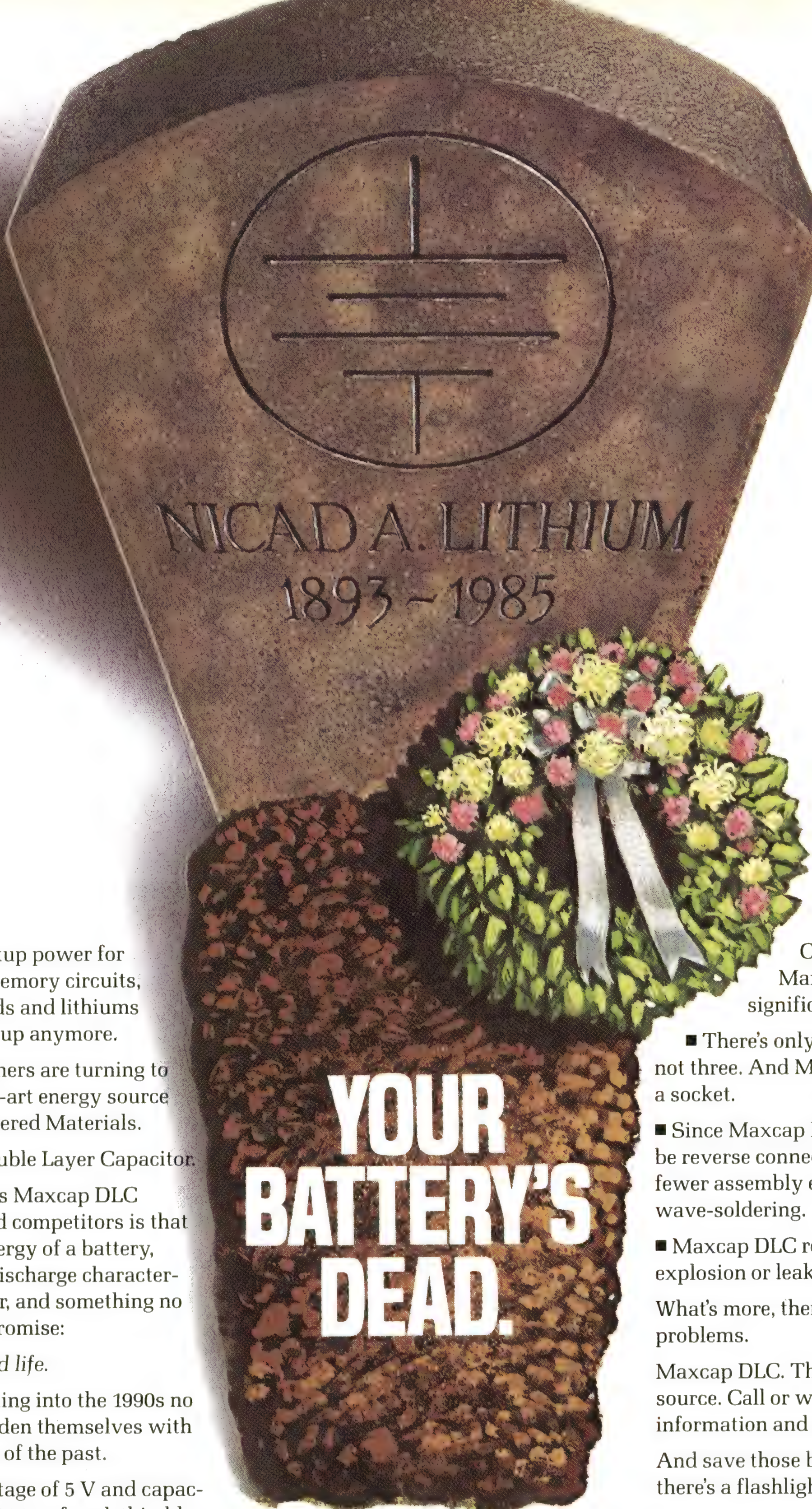

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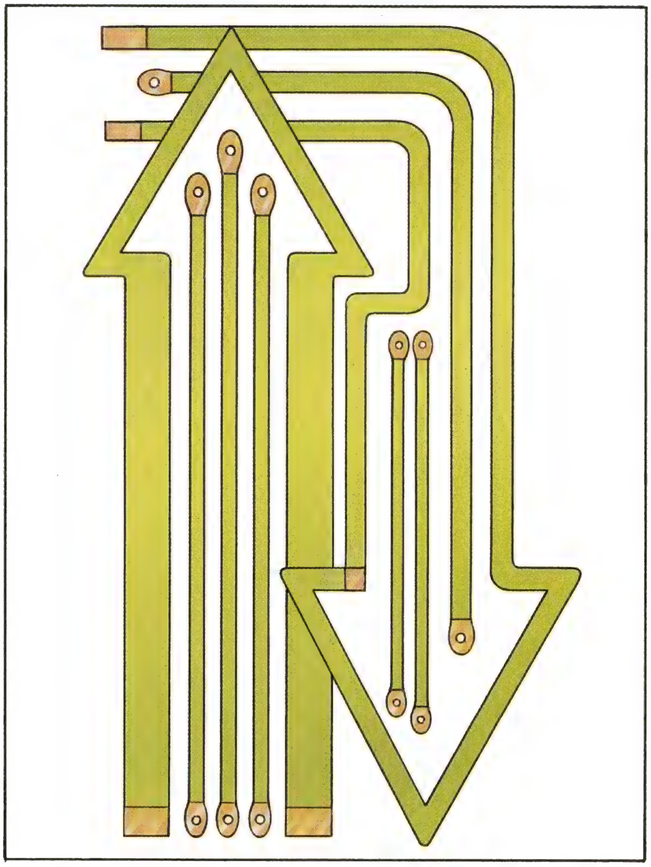

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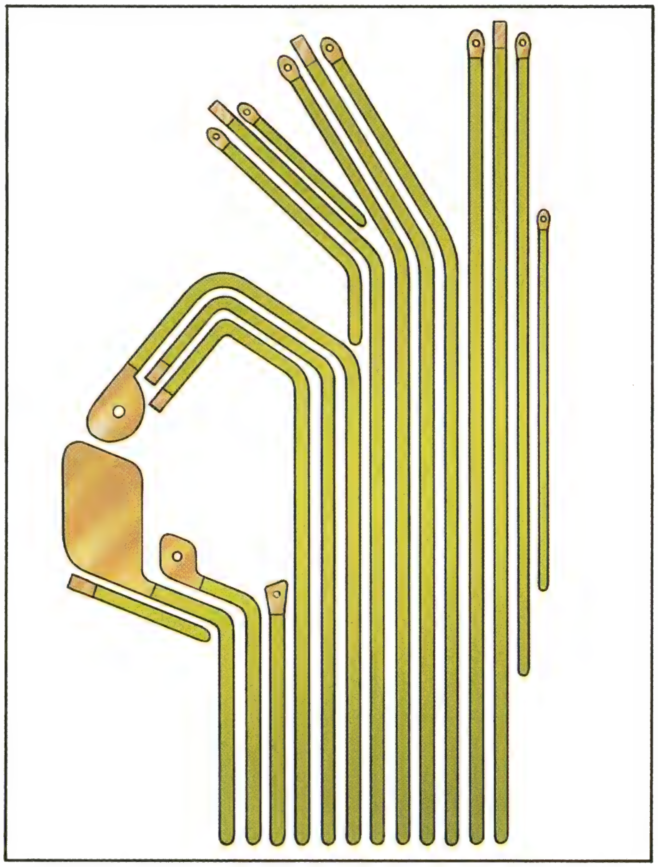

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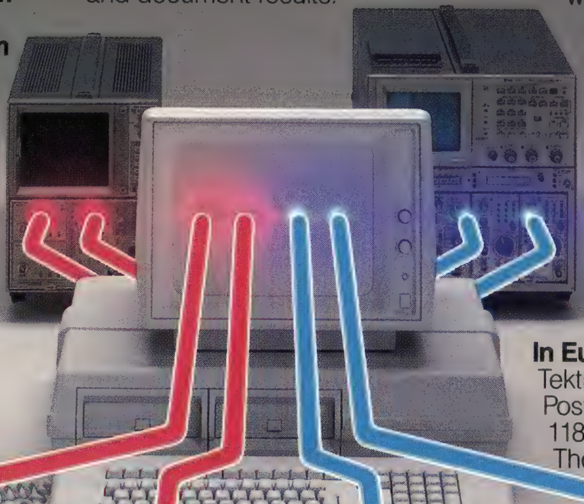

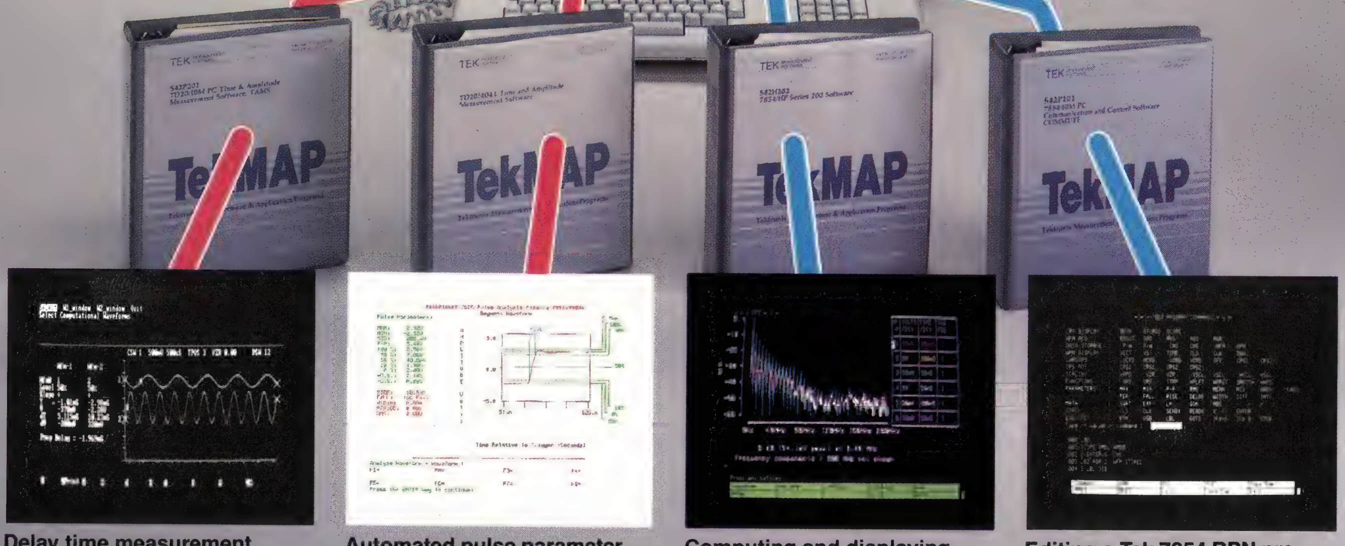

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Monolithic difference amp eases the design of a variety of circuits

The general-purpose INA105 monolithic difference amplifier can replace discrete op amps and resistors in a variety of circuits. Because the part's four resistors are closely matched, the chip offers better performance than that of discrete- or hybrid-component implementations.

R Mark Stitt, *Burr-Brown Corp*

You can use the INA105 precision difference amplifier to replace discrete op amps and resistors or a hybrid op amp/resistor network in a number of analog circuits, such as reference-voltage generators, instrumentation amplifiers, summing amplifiers, current sources, and absolute-value buffers. Like all monolithic circuits, the difference amplifier uses less pc-board real estate and delivers better temperature performance than do discrete-component implementations. The INA105 offers an extra advantage, however: The part's four resistors are closely matched, so you don't need to perform resistor matching.

One application for the monolithic difference amplifier is that of a reference-voltage generator in a unity-gain inverting amplifier. To obtain a precision ±10V reference, you connect the INA105 with a REF10 (zener-based) voltage reference, as shown in **Fig 1a.** In this instance, the INA105's offset and low-gain temperature drift add only about 2 ppm/°C to the reference's temperature drift.

To obtain a ±5V reference, connect the INA105 to REF10 as shown in **Fig 1b.** This configuration lets you operate a zener-based reference from dual supplies whose voltages are lower than the zener voltage. You can, for example, take advantage of the performance of a 10V zener reference when using ±9V power supplies.

By combining state-of-the-art op amps with the INA105, you can design a high-performance instrumentation amplifier **(Fig 2).** Resistors R_1 and R_2 set the gain of the instrumentation amplifier according to the transfer function

$$V_O = \left(1 + \frac{2R_2}{R_1}\right)\left(V_2 - V_1\right).$$

These resistors determine gain only, and you can achieve a high common-mode rejection ratio (CMRR) without precise resistor matching. The difference amplifier's operating errors are effectively divided by the gain of the input amplifiers. The instrumentation amplifier's overall performance is limited only by the input amplifiers.

In low-source-impedance applications, you can improve the instrumentation amplifier's noise, offset, and temperature-drift performance by using OPA37 bipolar op amps for the input stages. At source-impedance

By combining state-of-the-art op amps with the INA105, you can design a high-performance instrumentation amplifier.

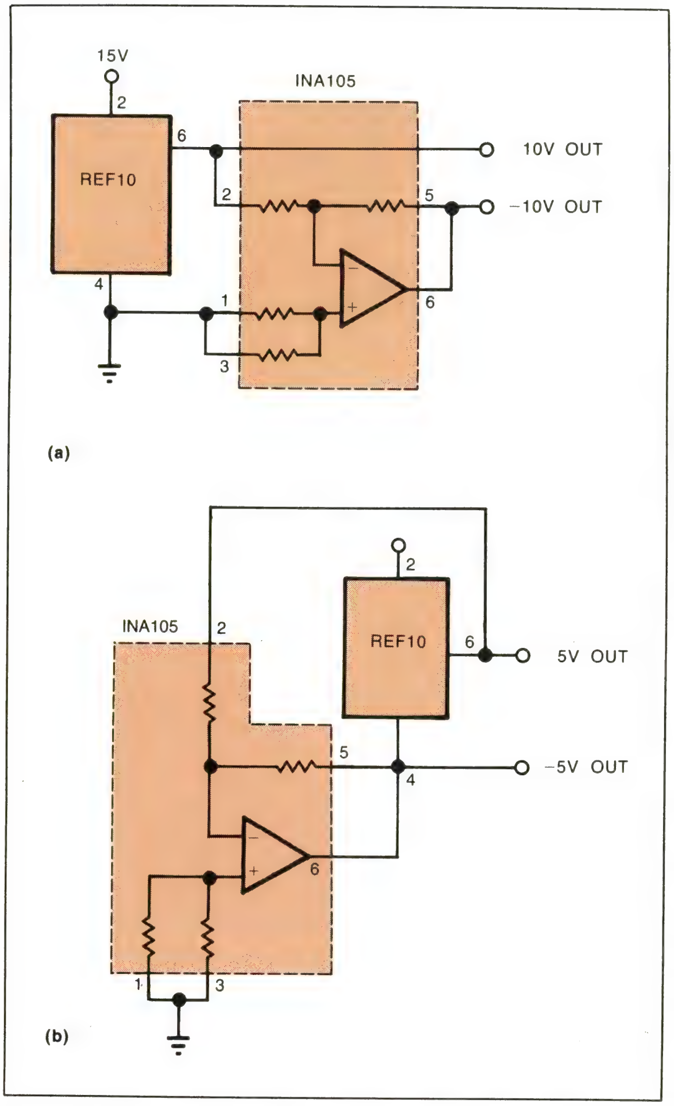


Fig 1—To develop precise reference-voltage generators, simply configure the INA105 as a unity-gain inverting amplifier. In the ±10V reference circuit (a), the INA105's low gain- and offset-temperature drifts add only about 2 ppm/°C to the reference temperature drift. In the ±5V reference circuit (b), you can operate the REF10 from supply voltages that are lower than the zener voltage.

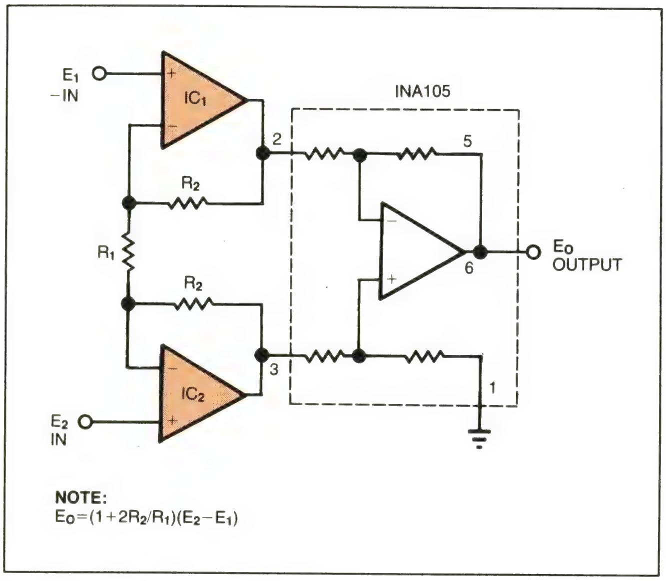


Fig 2—You can design a high-performance instrumentation amplifier by combining state-of-the-art op amps with the INA105. To realize low-noise performance in applications in which source impedance exceeds 10 kΩ, you should employ FET-type op amps in the input stages.

levels above approximately 10 kΩ, the bias-current noise of an OPA37 reacts with the input impedance and begins to dominate the noise performance of the instrumentation amplifier. To realize low-noise performance in these applications, you should use OPA111 FET-type op amps in the input stages. **Table 1** illustrates the performance of **Fig 2**'s instrumentation amplifier when it's set for a gain of 100. To construct an electrometer-grade instrumentation amplifier, use the OPA128 for a 75-fA bias current.

Further, if you drive the noninverting input resistors in parallel and ground one of the inverting input resistors, you'll have a precision gain-of-2 amplifier **(Fig 3a)**. Here, the INA105's resistors establish the circuit's 0.01% gain accuracy. More important than gain accuracy, however, is the gain temperature drift of 2 ppm/°C that results from the difference resistors' careful TCR (temperature coefficient of resistance) tracking.

You can use this precision gain block to extend the input common-mode range of an instrumentation amplifier without degrading either its gain accuracy or its gain drift vs temperature. For example, in **Fig 3b**, this gain-block technique extends the INA102 instrumentation amplifier's common-mode range from 5 to 7.5V. In contrast, in a conventional instrumentation amplifier, the drive voltage necessary to develop 10V at the output of difference amplifier IC_3 limits the input's common-mode range. Adding gain improves the circuit's common-mode range because the instrumentation amplifier's output no longer has to develop 10V.

If you apply signals separately to the noninverting input resistors of an INA105, the gain-of-2 block in **Fig 3a** becomes a precision summing amplifier. To obtain a summing amplifier with gain, simply add a pair of external resistors **(Fig 4)**. The inputs are summed at a gain proportional to the ratio of the external feedback

TABLE 1—INSTRUMENTATION AMPLIFIER PERFORMANCE

A_1, A_2	R_1 (Ω)	R_2 (Ω)	GAIN (V/V)	CMRR (dB)	I_B	NOISE (1 kHz) (nV/$\sqrt{Hz}$)
OPA37A	50.5	2.5k	100	126	40 nA	4
OPA111B	202	10k	100	110	1 pA	10
OPA128LM	202	10k	100	118	75 fA	38

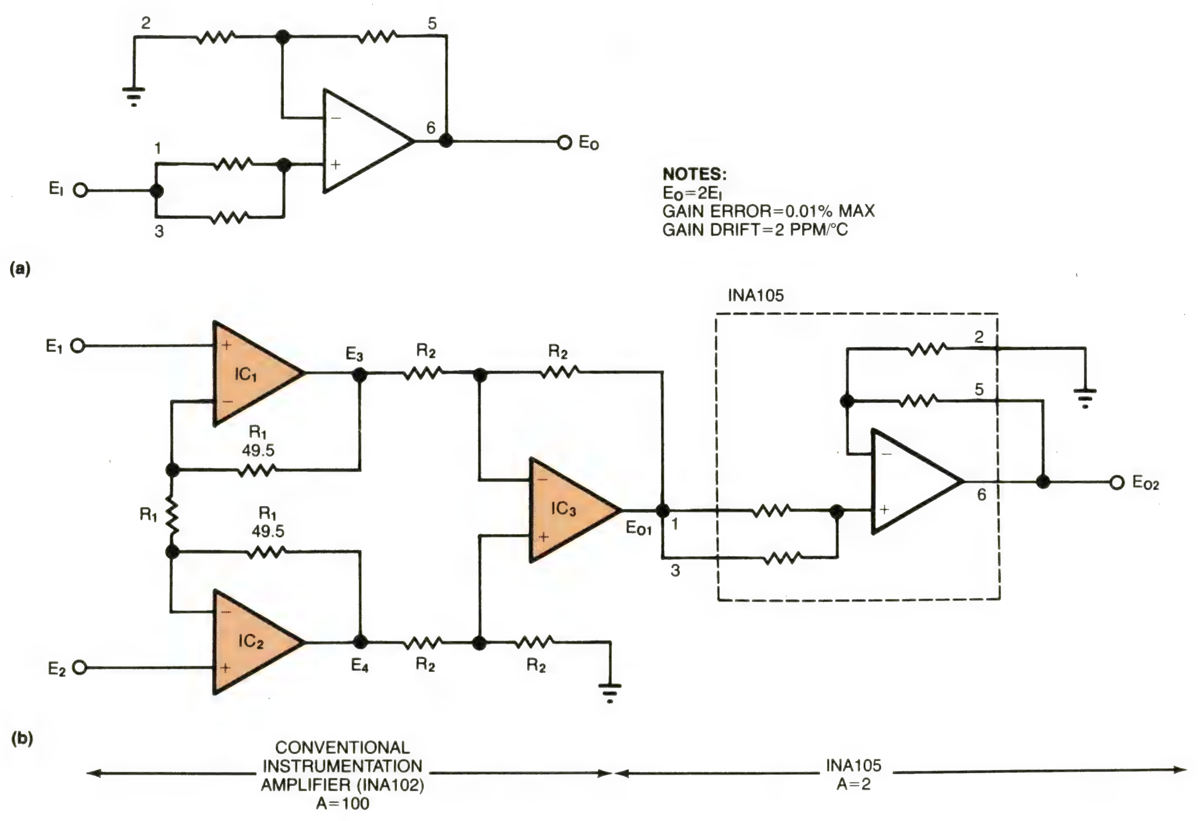


*Fig 3—**To develop a precision gain block,** simply configure the INA105 as a gain-of-2 amplifier **(a)**. By combining this gain block with an INA102 instrumentation amplifier **(b)**, you can increase the INA102's common-mode-voltage range by 50%.*

resistors. The internal difference resistors set the summation accuracy (0.01%), while the ratio accuracy of external resistors R_1 and R_2 determines the gain accuracy. Offset error will be equal to one half of the INA105 output offset, times the gain, which is determined by the external resistors.

The INA105 can also serve as a voltage-controlled current source, as shown in **Fig 5,** which depicts an enhanced version of the Howland current pump. The INA105's differential input capability makes the current source versatile: By grounding either input and driving the other, you can source or sink current from

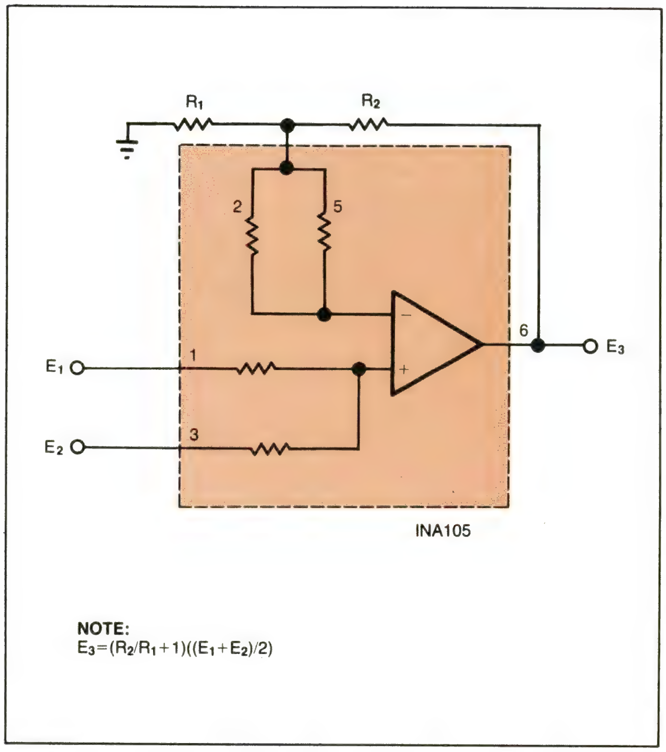


Fig 4—To develop a precision summing amplifier with gain, *connect a pair of external resistors (R_1 and R_2) to the INA105 and drive the INA105's noninverting inputs independently.*

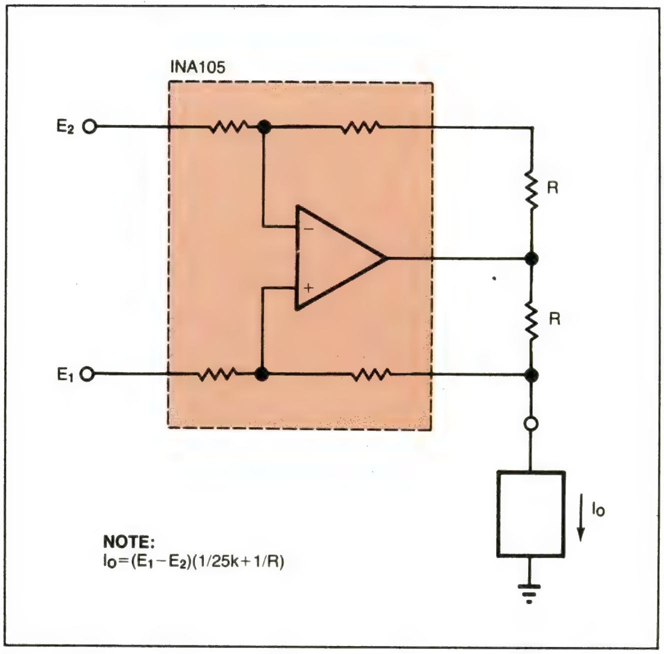


Fig 5—To source or sink current from either polarity of input voltage, *you can employ the INA105 in this enhanced version of the Howland current pump.*

either polarity of input voltage. If you drive both inputs simultaneously, the circuit will develop an output current proportional to the input-voltage differential.

The classical Howland current pump was difficult to implement because it required closely matched resistors and very accurate TCR tracking. The INA105, however, will let you implement the current pump easily; you simply add two external resistors. You still have to match the external resistors, of course, but you won't have to match them exactly. Because these external resistors work in conjunction with the INA105's 25-kΩ resistors, the matching requirement is modified by the ratio of external to internal resistance **(Fig 5).**

For external resistance values of 100Ω or less, 1% accuracy is adequate. Above 100Ω, you should trim the resistor connected to pin 5 to maintain high CMRR, thereby keeping the current source's output impedance high. You can approximate this output impedance by using the following expression:

$$Z_O = R'\left(10^{CMRR/20}\right),$$

where R′ equals the parallel combination of R and 25 kΩ, and CMRR is the common-mode rejection ratio of the INA105.

Current transmitter sinks and sources current

Because of its 20-mA output-current rating, the INA105 is also suitable for use as a 4- to 20-mA current transmitter, as **Fig 6a** shows. The transmitter circuit converts a 0 to 10V input to a 4- to 20-mA output. The OPA27 is configured as an inverting attenuator. It combines the 10V reference and the 0 to 10V input to develop a −0.2 to −1V signal range at the inverting input of the INA105.

By limiting the current pump's input to −1V—and, therefore, limiting the voltage across the 50.1Ω resistors to 1V—you can obtain output compliance of greater than 9V when the current transmitter is driving a grounded load. Unlike open-collector or open-drain designs, this current transmitter can both sink and source current.

To provide both buffering and gain for the current transmitter, you can add a pair of op amps at the transmitter's input **(Fig 6b).** As was the case with the instrumentation amplifier, the choice of bipolar or FET op amps depends on your application. When you use OPA27s on the input, this circuit will provide low-noise amplification, high common-mode rejection, and cur-

You can use a precision gain-of-2 block to extend the input common-mode range of an instrumentation amplifier without degrading its gain accuracy.

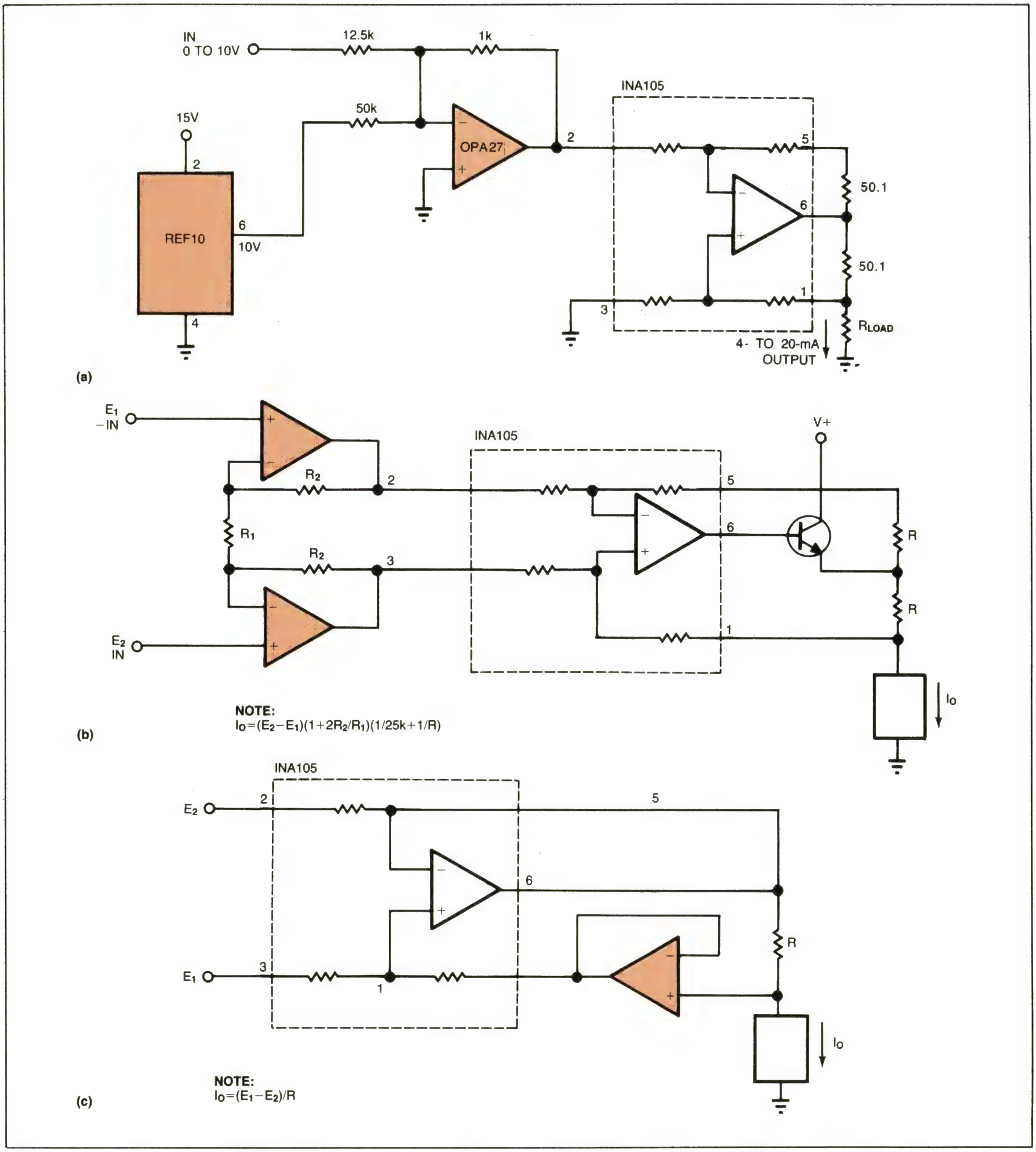


Fig 6—To design a 4- to 20-mA current-transmitter circuit, *use an OPA27 to sum the reference and use 0 to 10V signal inputs to develop a −0.2 to −1V signal range at the input of the INA105* ***(a)****. To provide both buffering and gain, add a pair of op amps at the input* ***(b)****. To compensate for temperature problems, add an amplifier to buffer the INA105's reference pin* ***(c)****.*

By grounding either of the INA105's inputs and driving the other, you can source or sink current from either polarity of input voltage.

rent-transmission capability for direct thermocouple inputs. For applications requiring high-level current-output capability, you can add an npn transistor at the output of the INA105, as in **Fig 6b.**

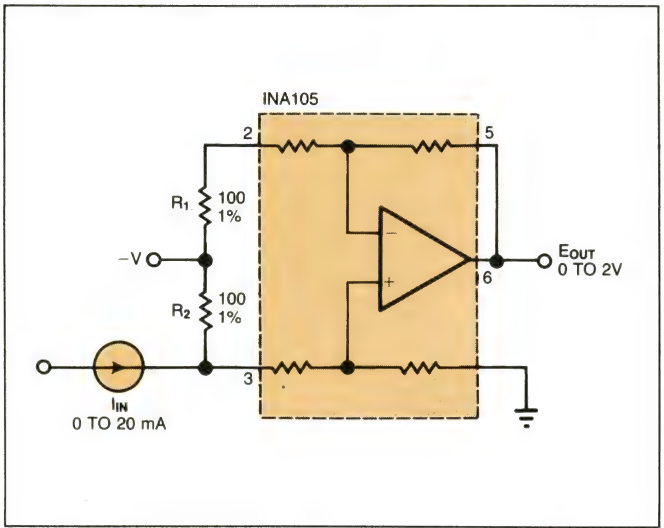


Fig 7—This current-receiver circuit offers compliance to either power-supply rail. *The second 100Ω resistor (R_2) preserves the input-resistance match of the INA105, maintaining high CMRR.*

When you implement the current pump, be sure to keep your external resistance values as low as possible. Large external resistances (greater than 250Ω) can decrease your circuit's CMRR, because even though the INA105's R_2/R_1 to R_4/R_3 ratio is trimmed to 20 ppm, the absolute match of the two sides (R_2/R_4, for example) is only about 1%. If you add two perfectly matched 250Ω external resistors, the resulting mismatch could be as much as 0.01%, lowering the CMRR to 86 dB.

In addition, as the value of the external resistors increases, TCR-tracking performance will suffer. If the external resistors' TCR is 100 ppm/°C, values exceeding about 500Ω will degrade the circuit's CMRR (and therefore its output impedance) over temperature. You can solve this temperature problem by adding an amplifier to the output of the INA105 in your current-transmitter circuit **(Fig 6c)**. The op amp will buffer the reference pin of the difference amplifier, eliminating any need for resistor matching.

Fig 7 illustrates a current-receiver circuit that has compliance to either power-supply rail. When you put a 100Ω sense resistor between the INA105 and the supply rail, the circuit's transfer function is $E_O=100I_I$, for E_O in volts and I_I in amps. Adding another 100Ω

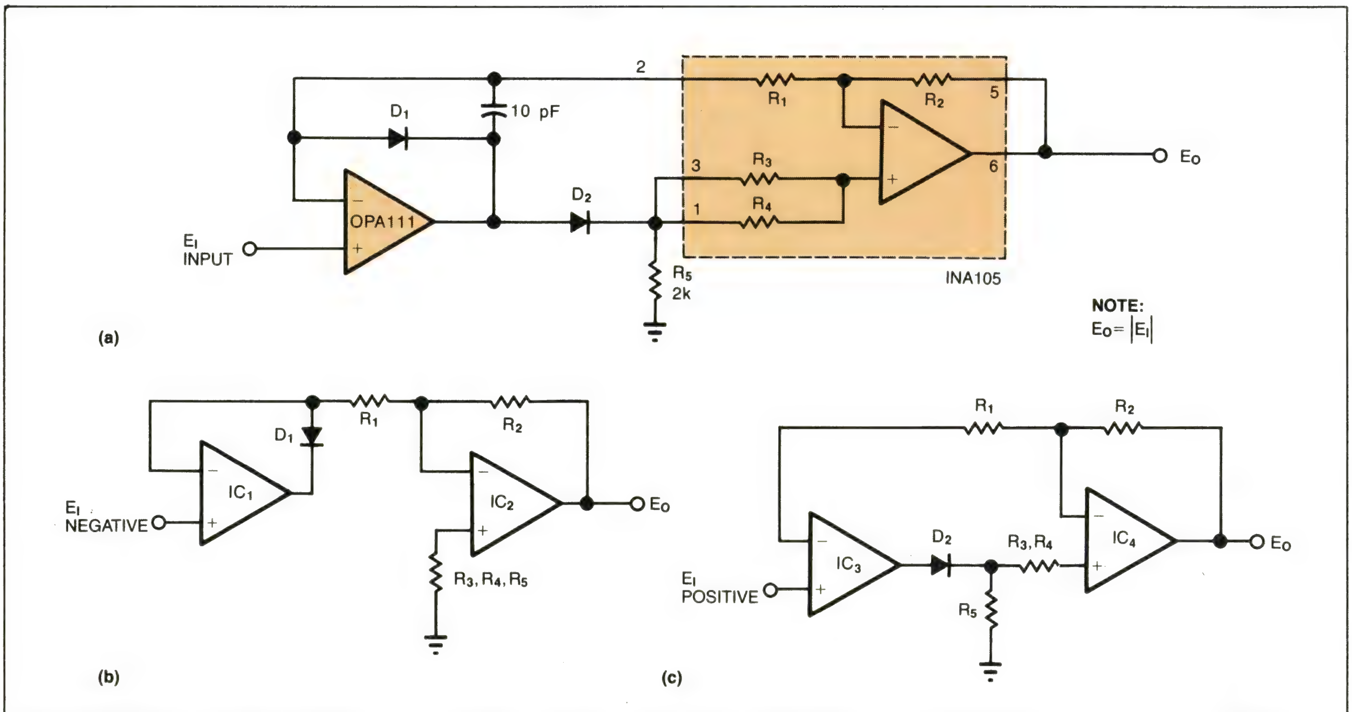


***Fig 8—By connecting a few components** to the INA105, you can configure the difference amplifier as a precision absolute-value buffer. The OPA111 in the buffer circuit **(a)** provides FET-type input characteristics. When the input signals are negative, the circuit functions as a unity-gain inverting buffer **(b)**. When the input signals are positive, the circuit functions as a unity-gain buffer **(c)**.*

Some difference-amplifier basics

In basic terms, a difference amplifier, such as the INA105 from Burr-Brown **(Fig A)**, is the combination of a unity-gain inverting amplifier and a gain-of-2 noninverting amplifier with a ½ resistor divider on that input. Therefore,

$$E_O = -E_{I1} + E_{I2},$$

where E_{I1} is the inverting input's voltage and E_{I2} is the noninverting input's voltage. If the signals at the inputs are equal, the signal at the output is zero. The difference amplifier responds to the difference between the signals at its inputs and rejects the common-mode signal.

The common-mode signal is the signal that appears on both inputs. Mathematically, it's expressed as

$$V_O = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right)V_2 - \frac{R_2}{R_1}V_1.$$

The INA105's 100-dB CMRR results from the 0.002% match of the R_4/R_3 ratio to the R_1/R_2 ratio. Because the resistors' TCR tracking is better than 2 ppm/°C, the part maintains an 86-dB min CMRR at 85°C.

When you're applying a difference amplifier, it's important to preserve the critical resistor matching. Any source impedance adds directly to the input-resistance values (at R_1 and R_3). Likewise, any wiring resistance adds directly to the precision-difference resistance at any of the resistors. A resistance of 5.0Ω will degrade the CMRR to 80 dB.

Because the resistors in the amplifier are carefully matched to preserve the $R_2/R_1 = R_4/R_3$ relationship, you should connect the INA105 as shown; don't interchange pins 1 and 3 or 2 and 5. If you were to switch R_3 and R_4, for example, the device would still be a difference amplifier, but its performance would suffer. If you were to switch pins 1 and 3, the ratio accuracies might be only 0.01% instead of 0.002%, and the circuit would experience increased temperature drift and thermal-feedback errors, in addition to CMRR problems.

Further, if you use the reference pin to trim the voltage offset, you must maintain the resistor ratios, thus preserving CMRR and gain accuracy. To maintain the resistor ratios, you can add a 10Ω resistor in series with both the reference and noninverting-input pins, as shown in **Fig B**. To realize 300 μV of offset adjustment, you can drive the offset point through a 499-kΩ resistor from the potentiometer.

The input common-mode range of a difference amplifier extends to the power-supply rails and beyond. To sense a transmitted current signal (such as a 4- to 20-mA signal) at one of the power-supply rails, put the current-sense resistor at the power-supply rail; this setup will let you take maximum advantage of the current transmitter's compliance. Unlike a conventional instrumentation amplifier—which can't function when its inputs are close to the power-supply rail, and thus requires you to restrict the common-mode range of the signal—a difference amplifier lets a sense resistor monitor the signal directly at the rail without your having to restrict common-mode range.

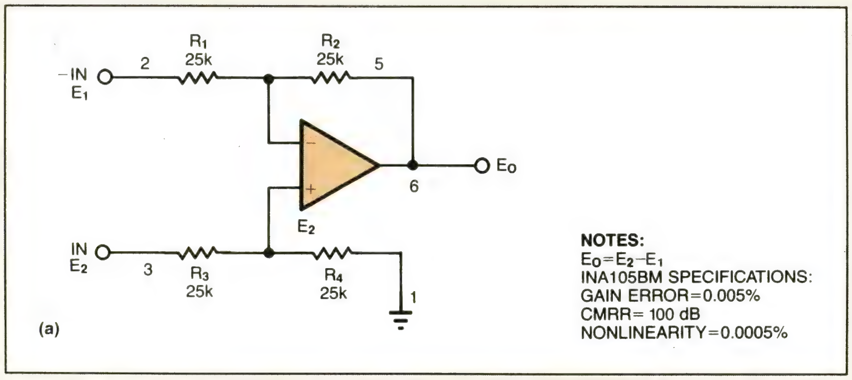


__Fig A—A difference amplifier__ such as the INA105 includes a unity-gain inverter, a gain-of-2 amplifier, and a pair of resistor dividers.

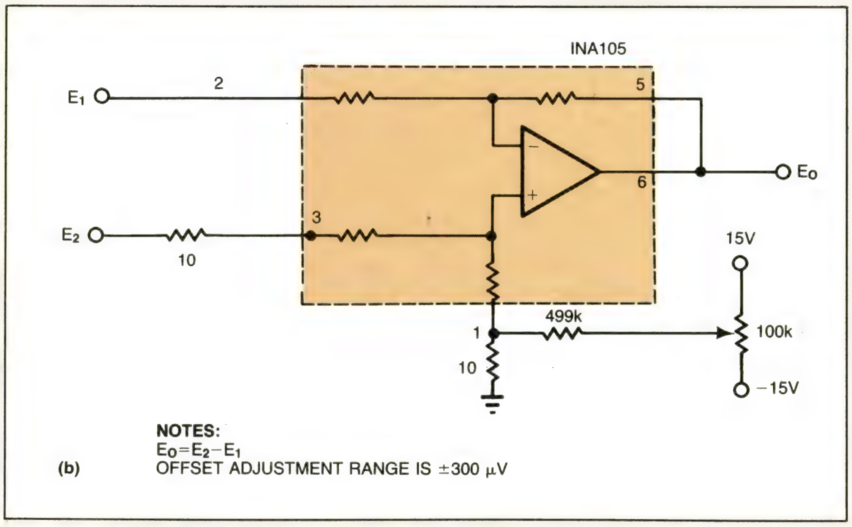


__Fig B—You can adjust__ the INA105's offset by using the circuit shown here.

You can implement an enhanced version of the Howland current pump simply by connecting two external resistors to the monolithic difference amplifier.

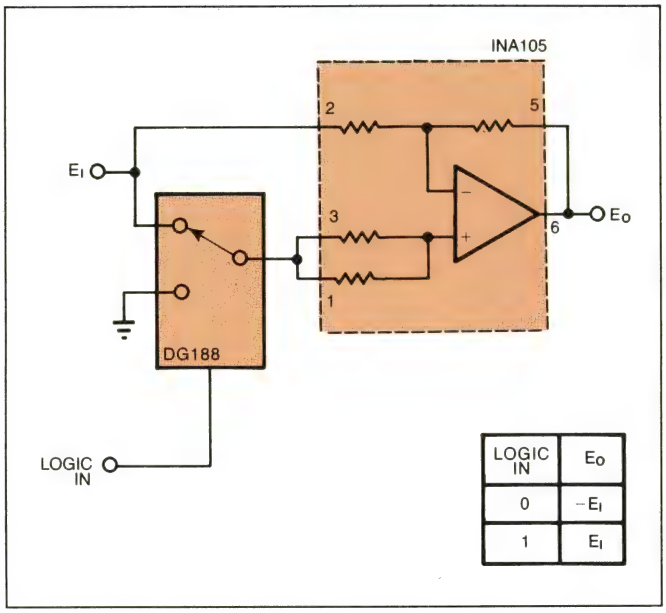


Fig 9—To control analog circuits with digital signals, *you can configure this unity-gain buffer as an amplifier with a digitally controlled gain of ±1. In this figure, the DG188 analog switch acts under logic control to connect the INA105's noninverting input to either the input signal or ground.*

resistor preserves the input resistance match of the INA105 and maintains high CMRR. Because 100Ω is small compared to the 25-kΩ resistors in the difference amp, a 1% tolerance for the 100Ω resistors is sufficient to maintain an 86-dB CMRR.

The 100Ω sense resistor in series with pin 2 lowers the amplifier's gain by about 0.4%, and the 50-kΩ input impedance at pin 3 shunts the 100Ω sense resistor and reduces its effective resistance by 0.2%. The 1% tolerance of the 100Ω sense resistor could make the current receiver's gain error as high as 1.6%. Although 1.6% gain error is adequate for many applications, you can improve the gain accuracy to 0.05% by using 100.6Ω resistors with 0.02% tolerance.

Design an absolute-value buffer

The monolithic difference amplifier is also useful in absolute-value signal processing. By connecting a few components to the INA105, you can configure the difference amplifier as a precision absolute-value buffer **(Fig 8a).** The OPA111 provides FET-type input characteristics. Because rectification diodes D_1 and D_2 are within the input amplifier's feedback loop, the amplifier's open-loop gain corrects for the diodes' forward-voltage drop. The buffer circuit's overall accuracy equals that of the INA105—0.01%.

When it has negative input signals, the circuit functions as a unity-gain inverter **(Fig 8b).** D_2 is reverse biased, and IC_1 pulls current through D_1 to equalize the voltage levels at the inverting and noninverting inputs. Because R_1 equals R_2, IC_2 simply acts as a precision unity-gain inverter, and E_O equals $-E_I$.

When the circuit's input signals are positive, D_1 is reverse biased, and the circuit functions as a unity-gain buffer **(Fig 8c).** IC_1 forces current through D_2 to establish a voltage at IC_2's input. This voltage, in turn, makes the voltage at IC_1's inverting input equal to the voltage at IC_1's noninverting input. Because no current flows into the inputs of either IC_1 or IC_2, the voltage drop across both R_1 and R_2 is zero, and the voltage at the output of IC_2 equals that at the input of IC_1.

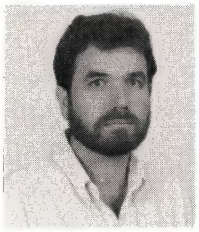
In an application in which you must use digital signals to control analog circuits, you can use the unity-gain buffer as an amplifier with a digitally controlled gain of ±1 **(Fig 9).** The DG188 analog switch acts under logic control to connect the INA105's noninverting input to either the input signal or ground.

For a logical-zero control signal, the noninverting input is connected directly to ground, and the circuit functions as a conventional unity-gain inverter. For a logical-one control signal, the INA105's noninverting input is connected to the input signal. Because the voltage across the amplifier's inputs is zero, no current flows through the input resistors, and the amplifier acts as a unity-gain buffer.

Errors contributed by the analog switch (a function of the on/off resistance ratio) are less than 0.01% in this example. The DG188 toggles in less than 150 nsec, so the circuit's settling time (to 0.01%) is less than 5 μsec.

EDN

Author's biography



Mark Stitt is an engineering manager at the Analog Div of Burr-Brown Corp (Tucson, AZ), where he manages a group that designs precision analog circuits. He holds a BSME degree from the University of Arizona and has worked at Burr-Brown for 18 years. In his spare time, Mark enjoys swimming, woodworking and gardening.

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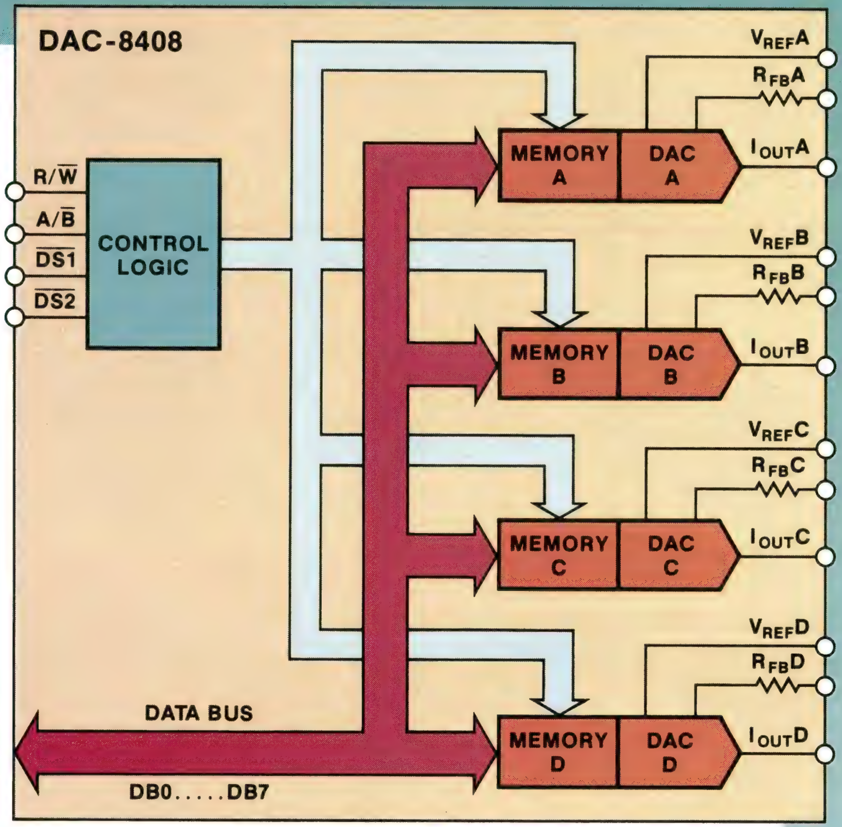

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CIRCLE NO 147

Build your own A/D converter for optimum performance

When you're faced with the task of solving an A/D-conversion problem, you can choose from a variety of off-the-shelf parts. In terms of performance, however, it might be better to build than to buy. By following some design guidelines, you can build your own high-speed 12-bit A/D converter.

Jim Williams, *Linear Technology Corp*

To economically achieve the best speed in an A/D converter, consider designing the part rather than buying it. Although you can choose from a variety of monolithic, hybrid, and modular SAR-based (successive-approximation-register-based) devices (the most popular technique employed in A/D-converter designs), such off-the-shelf solutions are generally either slower or more expensive than you'd prefer.

At the 12-bit conversion level, for example, the fastest monolithic devices spec conversion times of approximately 10 μsec. Modular and hybrid 12-bit converters can achieve 2-μsec conversion times, but such devices are expensive. By designing your own 12-bit A/D converter, you can build a device that solves both the conversion-speed and the cost problems.

Fig 1a shows a simple 12-bit, 12-μsec SAR converter. You'll find it easier to design faster converters if you understand this circuit's performance limitations. In **Fig 1b,** a clock signal (trace A) is applied to the 2504 SAR. On the rising edge of the start pulse (trace B), the SAR-D/A-converter combination begins to test each bit, starting with the MSB. Signal status at the LT1011's positive input (trace C) reflects this action. As shown, this waveform's voltage sequentially converges toward 0V as the SAR, D/A converter, and comparator provide servo control for the node.

The conversion-complete (CC) line (trace D) goes low after conversion of the LSB to signal the end of the sequence. The 7475 latch prevents the comparator from responding to input noise once the conversion is complete. This latch is reset at the next CC command.

Understanding some inherent limitations

When it comes to conversion speed, the D/A converter and the comparator are the major limiting factors in this circuit. For a worst-case, full-scale step, most bipolar D/A converters spec settling times of 150 to 200 nsec. In addition, the comparator's delay time comes into play. The clamp diodes limit excursions to speed comparator response, and the 820Ω resistor, which is

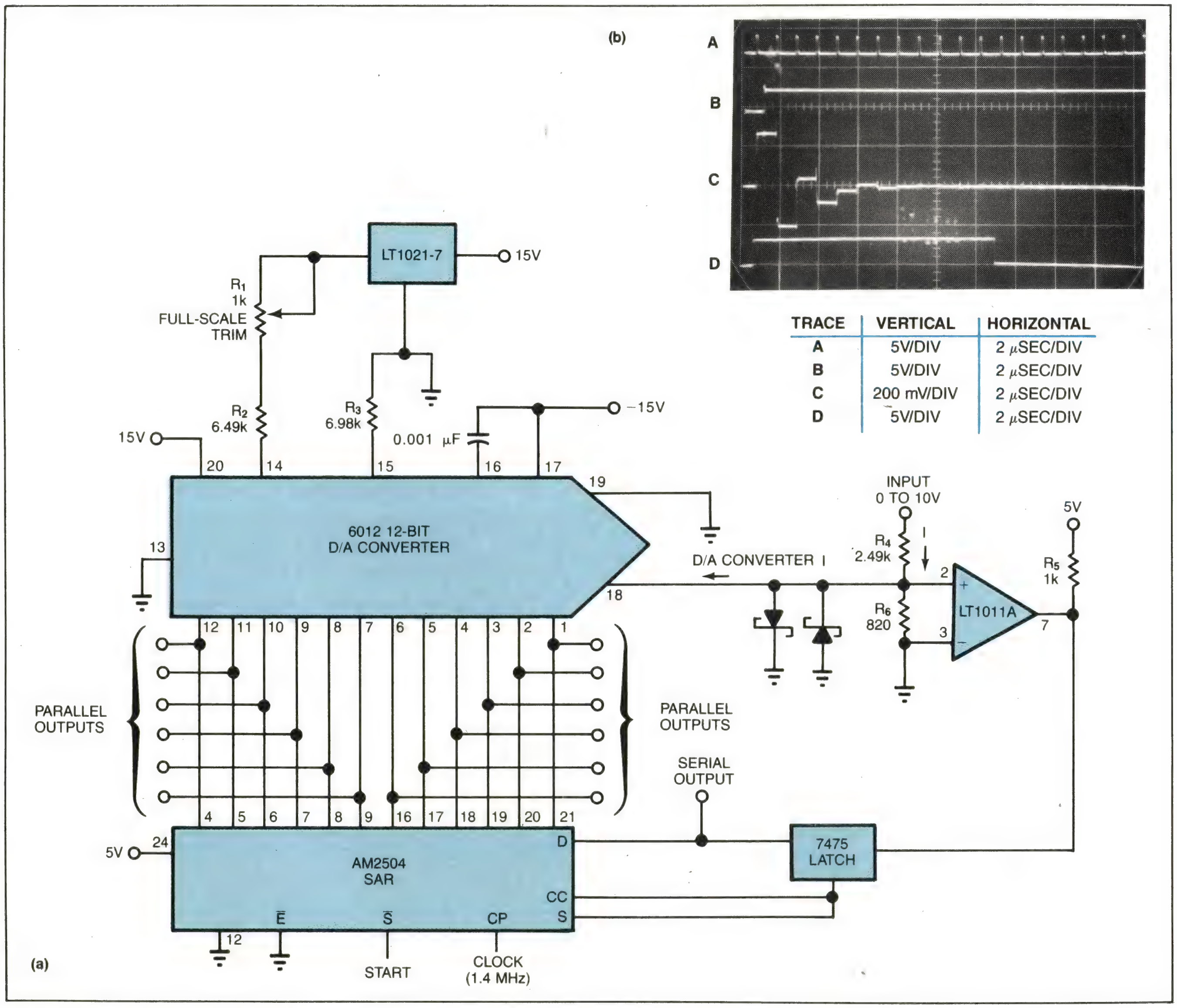
Successive-approximation A/D converters start with the MSB and work towards the LSB as they make each under/over decision.

connected to ground, shunts the D/A converter's output capacitance to speed comparator-D/A-converter node settling. Although this shunt degrades the voltage level per LSB available to the comparator, the LT1011's high gain compensates for that degradation.

In general, the circuit shown in **Fig 1a** is a fairly typical 12-bit SAR converter that features low cost and adequate speed. To realize higher conversion speeds, you'll need more sophisticated circuitry.

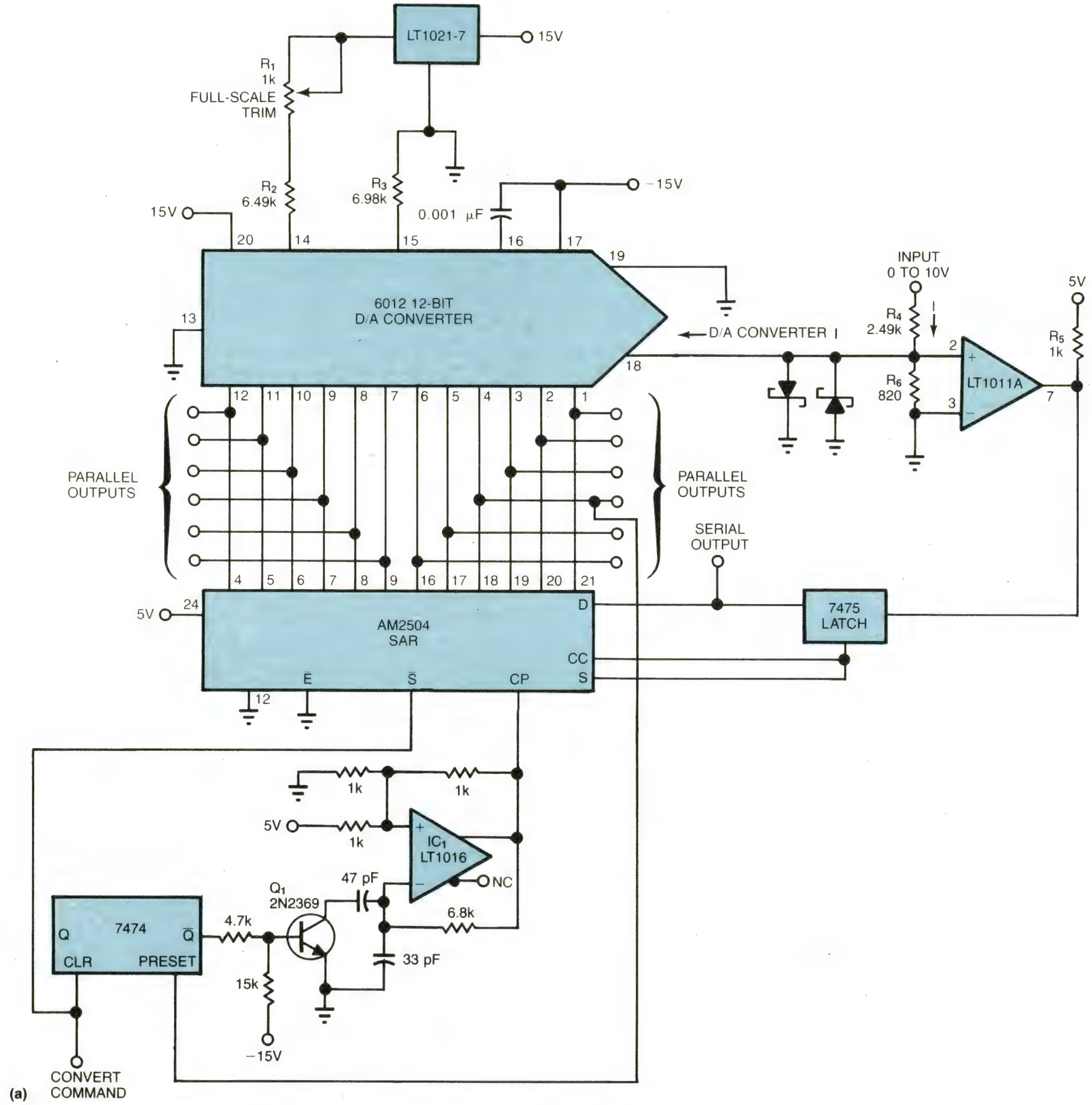
The circuit in **Fig 2a** uses a clock-modulation scheme to improve conversion speed. In this design, a 2-speed oscillator drives the clock terminal, CP. **Fig 2b** details circuit performance. A convert-command pulse (trace A) initiates the SAR routine. The pulse sets the 7474 flip-flop's $\overline{Q}$ output (trace C) high, which turns on Q_1. The 47- and 33-pF capacitors (part of oscillator IC_1's timing network) are now in parallel. IC_1's output pulses (trace B) drive the SAR's CP terminal.

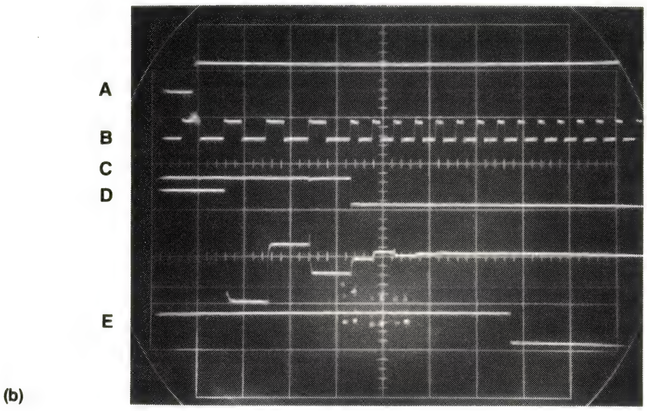
The flip-flop resets after conversion of the third MSB (trace C). Q_1 turns off, and the clock oscillator increases its frequency (trace B). The higher clock frequency reduces dwell time per bit at the comparator-D/A-



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	2 μSEC/DIV
B	5V/DIV	2 μSEC/DIV
C	200 mV/DIV	2 μSEC/DIV
D	5V/DIV	2 μSEC/DIV

Fig 1—Designing fast converters becomes easier *when you understand the performance limitations of this simple 12-bit SAR design* ***(a)****. In this case, both the D/A converter and the comparator limit circuit speed. The waveforms* ***(b)*** *reflect circuit operation.*





TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	1 µSEC/DIV
B	10V/DIV	1 µSEC/DIV
C	10V/DIV	1 µSEC/DIV
D	200 mV/DIV	1 µSEC/DIV
E	5V/DIV	1 µSEC/DIV

***Fig 2—You can improve conversion speeds** by using a clock-modulation scheme **(a)**. The circuit operation **(b)** shows that the flip-flop resets after conversion of the MSB bit (trace C), and oscillator frequency increases (trace B).*

Even when speed is not a prime design consideration, you may save money by building rather than buying an A/D converter.

converter junction (trace D), thereby decreasing total conversion time. As shown, the conversion-complete pulse (trace E) drops low 6.5 μsec after the convert-initiation command.

Although this clock-modulation approach significantly improves conversion speed, it does nothing to reduce the comparator's contribution to delay time. One solution to this problem is, of course, to use a faster comparator. But although the use of a faster comparator is a viable option at the 8-bit (or even the 10-bit) level, it causes problems at the 12-bit level.

For example, you could use an LT1016 (a 10-nsec device) in place of the slower (150-nsec) LT1011 to increase speed. If you do, however, you'll have to sacrifice available gain. The LT1011 has a minimum gain of 200,000, but the LT1016 specs a gain of only 1400. For a 10V full-scale A/D conversion, the LSB size is as follows:

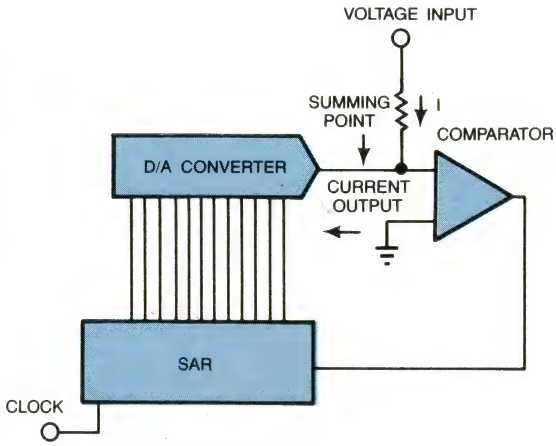
$$10V \div 4096 \text{ steps} = 2.44 \text{ mV}.$$

The successive-approximation technique

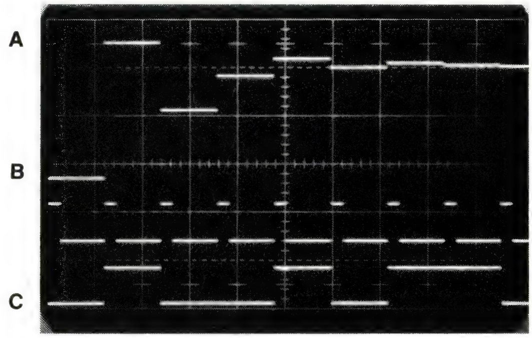
Use of the successive-approximation conversion technique probably dates to the invention of the weighing scale. In fact, you can most easily visualize this conversion technique by considering the operation of a beam balance.

With the beam balance, you determine an unknown weight held in one pan by successively placing standard weights in the other pan. The balance makes overweight/underweight decisions as you successively try standard weights (or combinations thereof) in a logical sequence to balance the scale.

Successive-approximation A/D converters start with the MSB and proceed towards the LSB after they make each under/over decision. Operation is straightforward (**Fig A**). Trace A shows the summing-node response as the converter, under instructions from the clock-driven successive-approximation logic (trace B), tries different bit weights. Trace C illustrates the comparator's decisions. Note how the summing point sequentially converges towards 0V—the analog of null in a beam balance.



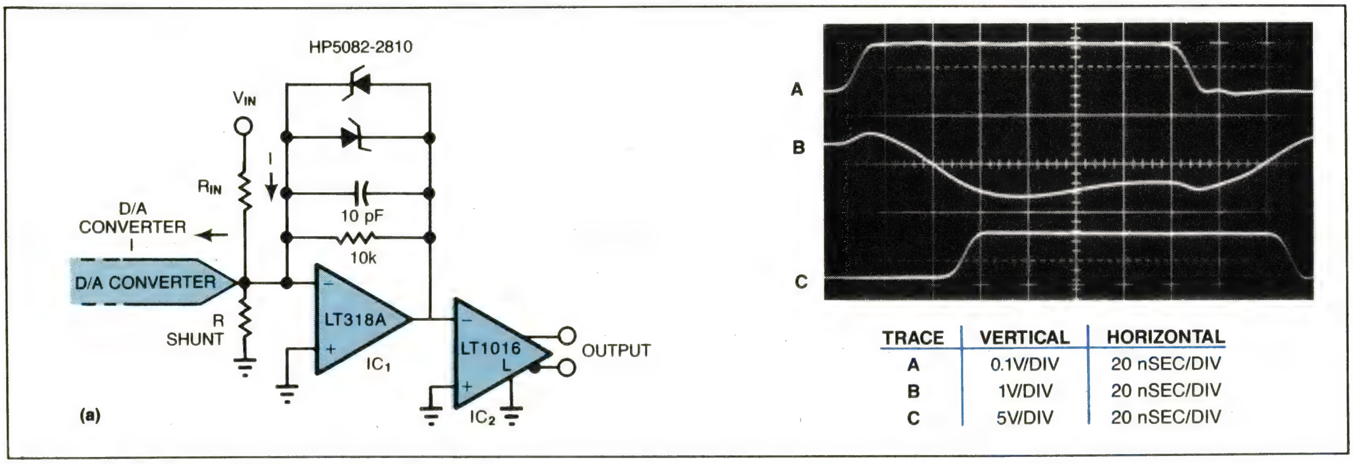
(a)



TRACE	VERTICAL	HORIZONTAL
A	0.1V/DIV	20 μSEC/DIV
B	5V/DIV	20 μSEC/DIV
C	5V/DIV	20 μSEC/DIV

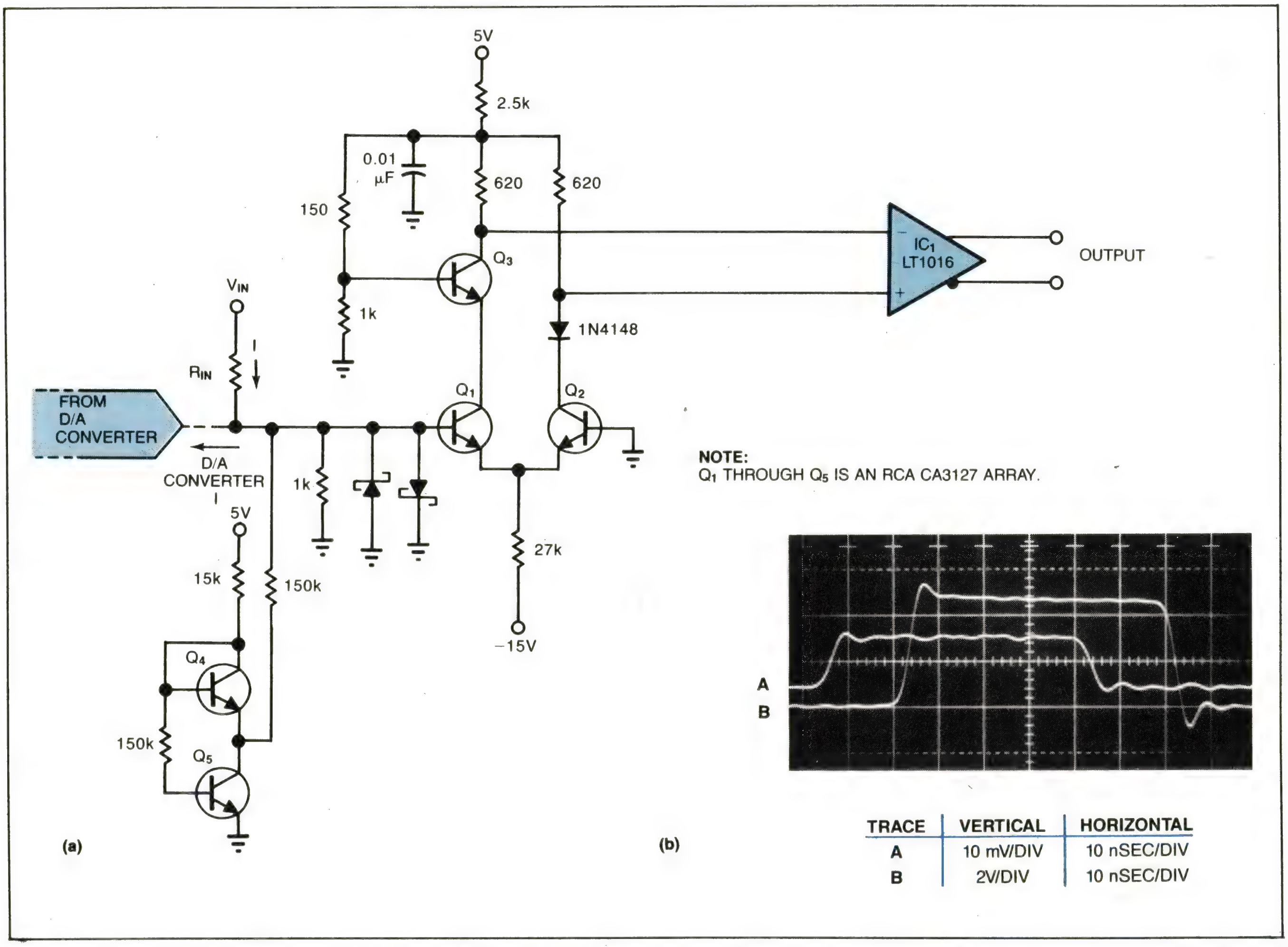
(b)

***Fig A—Operation is straightforward** in a SAR converter. As the converter, under control of the clock-driven SAR logic (trace B), tries different bit weights, the summing node response (trace A) sequentially converges towards 0. Trace C shows the comparator's decisions.*



TRACE	VERTICAL	HORIZONTAL
A	0.1V/DIV	20 nSEC/DIV
B	1V/DIV	20 nSEC/DIV
C	5V/DIV	20 nSEC/DIV

Fig 3—You can solve comparator gain problems *by using a simple preamplifier circuit* ***(a).*** *Although this is a fairly simple circuit, you can realize conversion times in the 3- to 5-µsec range* ***(b)*** *by using it in place of the LT1011 comparator.*



TRACE	VERTICAL	HORIZONTAL
A	10 mV/DIV	10 nSEC/DIV
B	2V/DIV	10 nSEC/DIV

Fig 4—To minimize conversion times even further, *you can use high-frequency transistors to design a faster preamplifier* ***(a).*** *A look at the circuit's operating waveforms* ***(b)*** *shows that the circuit output (trace B) switches in 15 to 20 nsec.*

To increase conversion speed, you must place a gain stage before the comparator.

To switch a full TTL-output level with ½LSB overdrive (1.22 mV), the comparator must have a minimum gain as follows:

$$5V \div 1.22\ mV = 4098.$$

Given this gain requirement, the comparator clearly requires assistance. In addition, the shunt resistor at the D/A-converter output reduces the input signal, making the conversion task more difficult. Finally, comparator speed will suffer with such a low-level overdrive.

You can solve the gain problem by placing a gain stage in front of the comparator. Although this scheme adds delay, it provides the needed overdrive for the comparator.

Fig 3a shows a simple preamplifier circuit. The preamp-comparator combination provides adequate gain (typically 4 to 10) and an overall response time of 40 to 50 nsec. IC_1 is configured as an amplifier bounded by Schottky-diode clamps. The diodes improve response time by keeping IC_1 out of saturation when summing-point overdrive is excessive. The 10-pF ca-

Specifying the D/A converter

In choosing a D/A converter for use in SAR-based A/D-conversion applications, you should remember that speed is often important and that the D/A converter is the slowest part of the A/D converter. The selection process therefore requires careful consideration.

Given the high speed inherent in bipolar current-mode D/A converters, such devices are popular. You still have to specify carefully, however. The output capacitance of CMOS D/A converters—in the 100- to 150-pF range—can excessively extend summing-node settling times. Of course, monolithic bipolar D/A converters, whose output capacitance is about 30 pF, settle faster. Voltage-mode D/A converters, on the other hand, are unpopular candidates for SAR applications. They aren't required to achieve summing action, and they are substantially slower than current-output types.

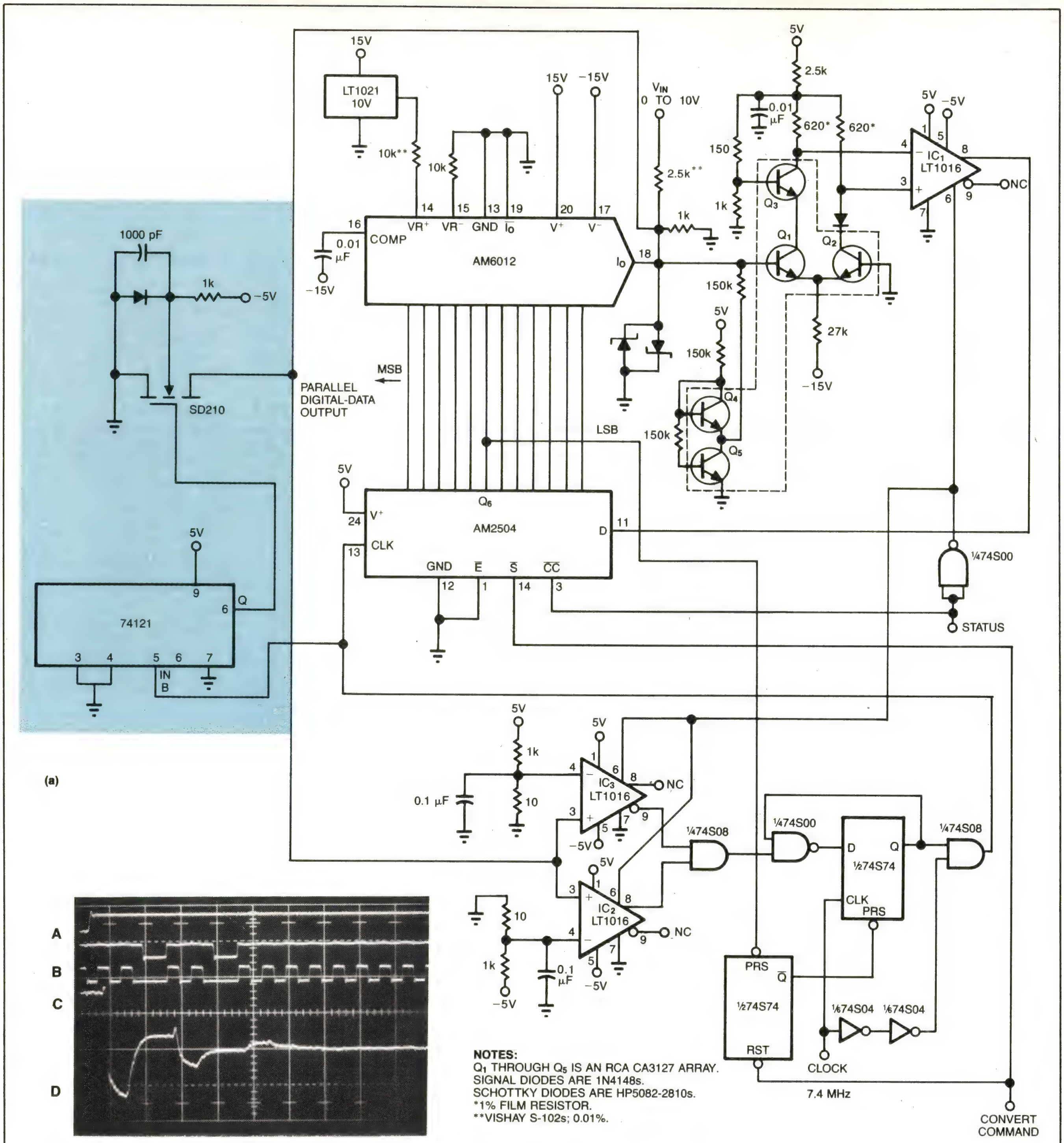
Extrapolate settling time

Settling-time specs for D/A converters are usually quoted for full-scale transitions. Smaller bit changes take less time, so you can extrapolate from full-scale settling time when you consider the D/A converter's effective settling time per bit in an A/D-conversion application. Unfortunately, the complex internal dynamics of a D/A converter rules out simple straight-line calculations; 1 LSB will not settle in 1⁄12 of full-scale time in a 12-bit unit.

For moderate speeds, you can assume that each bit transition will require the full-scale settling time. This conservative approach will never get you into trouble, but it will almost certainly guarantee slower-than-necessary D/A-converter performance. The best way to find out just how far you can push the D/A converter's settling-time specs in an SAR application is to consult the manufacturer. You can also measure the settling time under conditions that reflect the application environment. (For circuits that you can readily adapt to measure D/A-converter settling time, see "Settling-time measurements demand precise test circuitry," EDN, November 15, 1984, pg 307.)

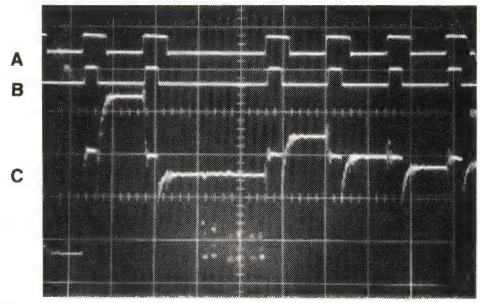
Considering the variety of D/A converters available, each with individual termination requirements, measurement results will vary considerably. In addition, the dynamics of D/A-converter types can vary substantially among manufacturers. It is possible, however, to provide some guidelines on what to expect. For example, the popular 565A, with a full-scale settling time of 250 nsec into 0Ω, can achieve a per-bit effective settling time of 110 to 150 nsec with careful design techniques.

Speed is not the only concern. A D/A converter's dc specifications translate directly into A/D-converter error terms. Linearity, drift, accuracy, and other dc terms contribute on a 1:1 basis to the converter's error characteristics. Monotonicity contributes as well. In a worst-case situation, a nonmonotonic D/A converter will cause an A/D converter to miss some output codes under certain input conditions.



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	200 nSEC/DIV
B	10V/DIV	200 nSEC/DIV
C	10V/DIV	200 nSEC/DIV
D	200 mV/DIV	200 nSEC/DIV

(b)



(c)

TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	100 nSEC/DIV
B	20V/DIV	100 nSEC/DIV
C	50 mV/DIV	100 nSEC/DIV

*Fig 5—**Primary speed-enhancing features** in this 12-bit SAR converter **(a)** include a closed-loop clock-control scheme and active summing-node clamping. Using a closed-loop clocking scheme, the circuit achieves a 1.9-μsec conversion time **(b)**. When you include the active summing-node clamp circuitry (the shaded portion of **a**), circuit conversion time is 1.8 μsec **(c)**.*

By combining closed-loop clock control with active summing-node clamping, you can enhance conversion speeds.

pacitor (a typical value in this case) compensates for the D/A converter's output capacitance. The capacitance value is application dependent, so you should use a value that provides the best amplifier damping. The feedback resistor (10 kΩ in this example) is selected for best gain-bandwidth performance.

As **Fig 3b** shows, a test input pulse (trace A) causes IC_1's output to slew through 0V (trace B), developing a negative bias level at IC_2's input. After a 10-nsec delay, IC_2 generates a clean TTL output (trace C).

Despite its simplicity, this circuit can significantly improve comparison speed. Use it in place of the LT1011 in **Fig 2a,** and you can realize conversion times in the 3- to 5-μsec range. If these conversion times are still too slow, you can use high-frequency transistors (at the GHz level) and design a faster discrete preamplifier **(Fig 4a)** to drive the LT1016 comparator.

In this cascoded differential amplifier, Q_4 and Q_5 provide bias-current compensation for Q_1's base current. **Fig 4b** illustrates how the circuit performs when you apply a test input signal (trace A). As shown, the LT1016's output (trace B) switches in 15 to 20 nsec. The LT1016 causes about 10 nsec of this delay; the preamp contributes the rest.

Preamplify for better speed

You can put this discrete preamplifier to good use in a high-speed 12-bit SAR converter (Fig 5a). Closed-loop clock control and active summing-node clamping are the primary speed-enhancing features. This circuit will perform a full 12-bit conversion in 1.8 μsec—about the practical limit with off-the-shelf components.

Conceptually, this circuit is similar to that in **Fig 2a.** However, the high-speed discrete preamplifier replaces the LT1011, and digital logic controls the clock speed. In this instance, the clock rate accelerates after conversion of the fifth MSB. During conversion of the upper four bits, a closed loop controls the clock rate to maximize overall speed.

The closed loop monitors conditions at the comparator-D/A-converter summing node. If the summing-node voltage excursion is greater than ±50 mV, the SAR operates at the maximum clock rate. If the excursion at the node is less than ±50 mV, the loop retards the clock rate to provide adequate settling time. The clock loop enhances conversion-time performance by not waiting for the bits that won't settle within ±50 mV. IC_2 and IC_3 form a high-speed window comparator that provides digital summing-node information to the clock logic.

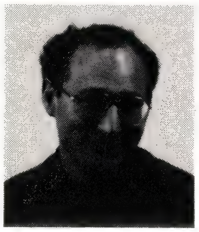
Fig 5b details the performance of the closed-loop clocking scheme (the circuit in **Fig 5a** minus the shaded portion). Trace A is the convert command, and trace B shows the gated output of the IC_2-IC_3 window comparator. The comparator's output state controls the clock line (trace C). Trace D depicts summing-point activity. The window comparator's decision controls the per-bit dwell time. After the fifth bit, the SAR's Q_6 line instructs the clock logic to run at maximum speed. Under these conditions, the circuit achieves a 1.9-μsec conversion time.

Converting still faster

To achieve the previously mentioned 1.8-μsec conversion time, include the 74121 one-shot and associated circuitry (the shaded portion of **Fig 5a).** These components form an active clamp at the comparator-D/A-converter summing node. Each time the SAR receives a clock pulse (trace A in **Fig 5c),** the 74121 generates a 30-nsec pulse (trace B). This pulse turns on the FET and shunts the summing node (trace C) to ground. The FET's low on-resistance discharges the D/A converter's 30-pF output capacitance for 30 nsec to reduce the converter's settling time. Each SAR-conversion step resets the summing node to 0. When the one-shot changes state, the node settles to its final value. This active clamping technique provides about a 10-nsec/bit savings in conversion time.

The 1.8-μsec conversion time provided by the circuit in **Fig 5a** approaches the practical limit for a 12-bit SAR converter. The effective D/A-converter settling time is about 100 nsec/bit. Comparator/preamp delay is about 20 nsec/bit, and SAR chip delays are about 25 nsec/bit. **EDN**

Author's biography



Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

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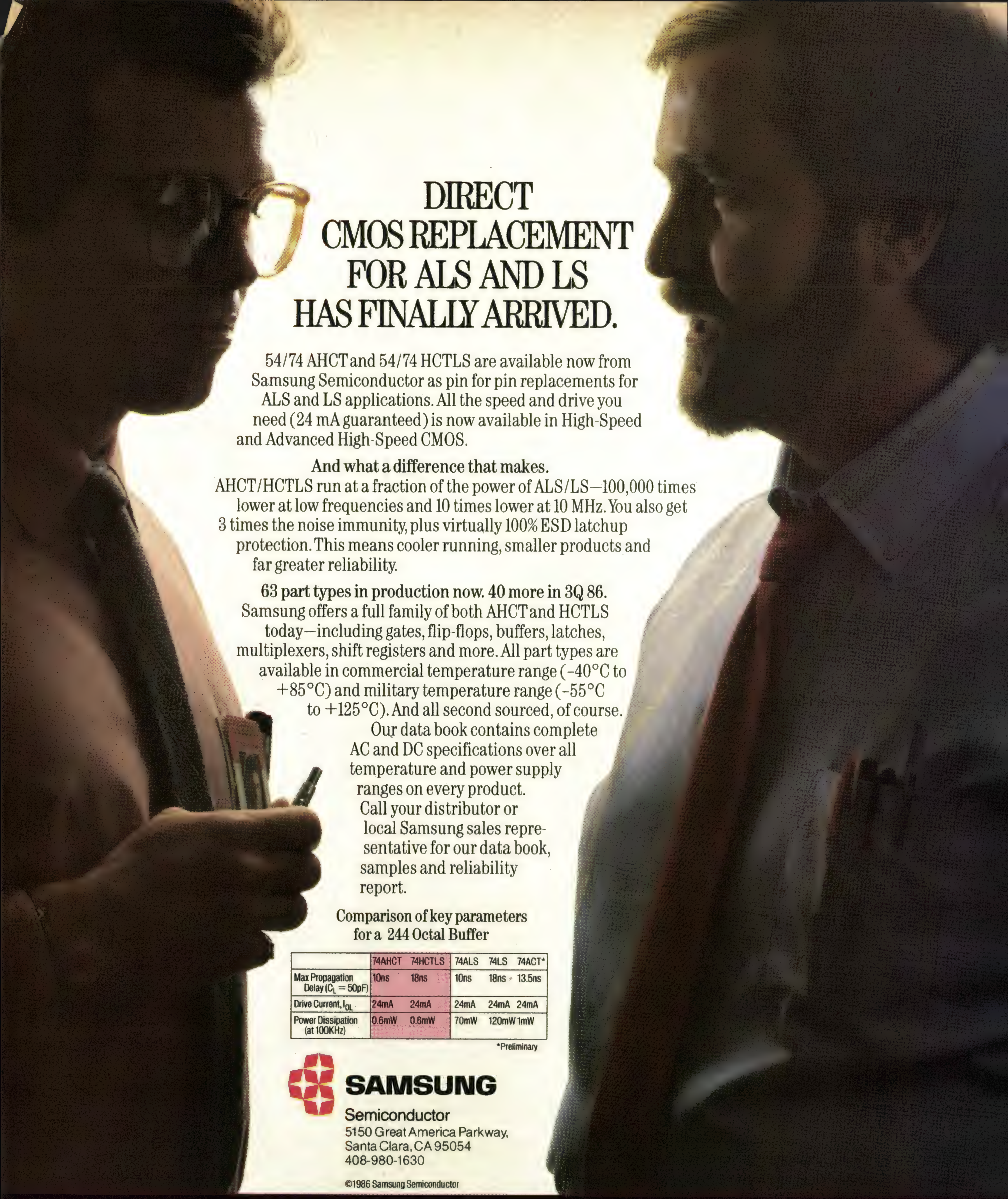

Static-RAM size adapts to your standard-cell design

Typical standard-cell layout packages offer components like static RAMs in only one size. Now, however, you can include in your design a static-RAM chip whose size you can adapt to your needs. All you need to lay out the static RAM are definitions of your processing technology, your RAM's size, and your I/O-pin requirements.

Abed W Mougharbel and Thomas D Housten,
RCA Solid State Division

To implement many designs in a standard-cell technology, you must be able to include not only MSI and SSI components in your chip, but also such elements as RAMs, ROMs, and multipliers. A structure like a RAM varies from one design to the next, however, so you must know how to adapt a single standard RAM cell to meet your design's requirements. Such knowledge can be incorporated into software that preserves the principal advantage of standard-cell use—short design time.

In your standard-cell designs, you can isolate the RAM or ROM and place and route the memory as a block that's separate from the rest of the layout. If you lay out the memory block by hand, though, you defeat

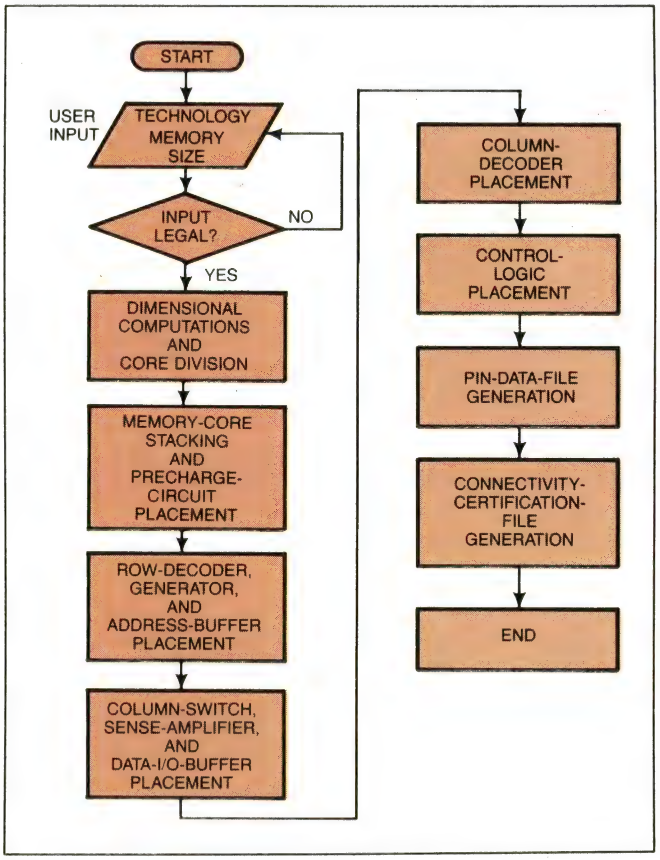

Fig 1—Once you have specified the size of your RAM *and the processing technology that you are using, the XRAM package carries out all the other steps in this flowchart automatically.*

Splitting the memory core brings the overall aspect ratio close to one and equalizes the amount of current drive that the column and row decoders require.

the purpose of using the standard-cell approach. Instead, you should use software that can automatically lay out simple standard cells, vary the size of the blocks, and connect those blocks to the rest of the IC.

Such software is available in the form of the XRAM (expandable RAM) package, which automatically generates and lays out small static RAMs. Within the program's limits, you can adjust the size of the RAM to suit your needs. Once you have created your RAM, you can use the Multi-Port 2-Dimensional (MP2D) standard-cell router **(Ref 1)** to connect the static memory to the rest of the chip. Both the XRAM design package and the MP2D router are a part of the Fastrack semicustom-design system. (The **box,** "Design package supervises program interaction," details how the parts of the standard-cell design package fit together.)

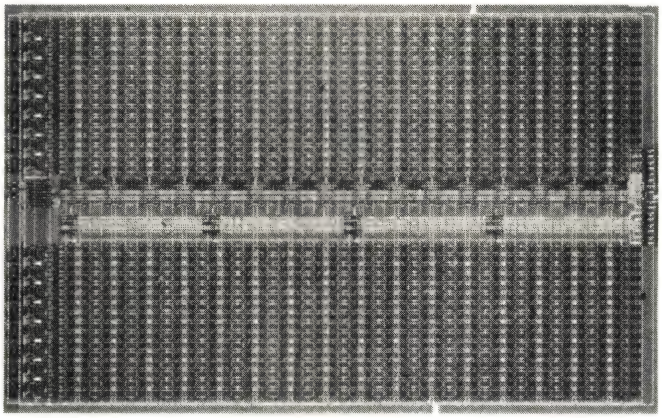

Fig 3—The XRAM program created the design *for this 64-word×16-bit static RAM. The subchip specs 60-nsec read and write cycle times, an operating current of 350 μA per bit, and a standby current of 1.5 μA per bit.*

Algorithm sees RAM parts as rectangles

The XRAM package uses a box-placement algorithm to lay out custom static RAMs. This algorithm views each part of a RAM as a rectangle, which the program characterizes with a fiducial coordinate, a length, and a width. The layout program calculates the Cartesian coordinates of the region in which it will place a rectangle before actually placing it. You must specify the interface requirements for the RAM before you begin the layout; the program can then connect all signals automatically.

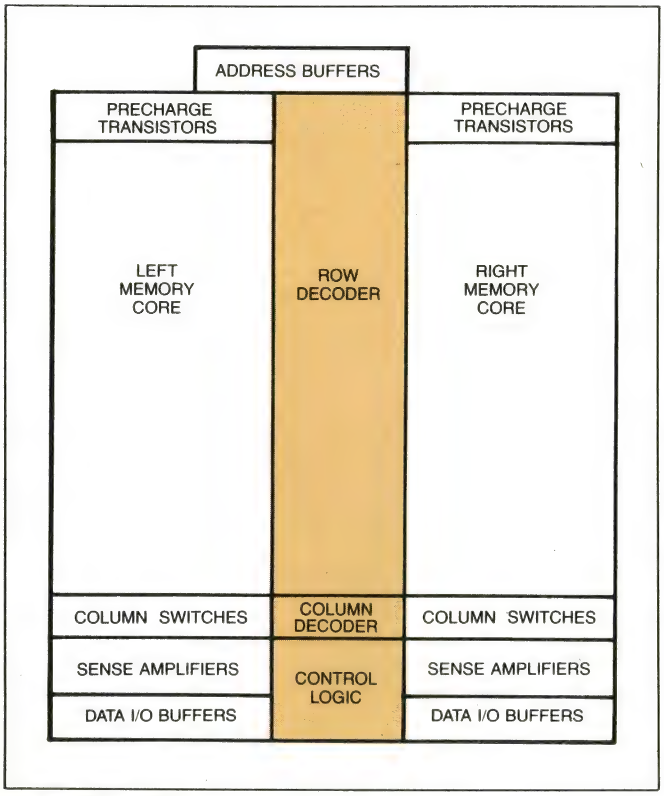

Fig 2—The XRAM program splits the memory core *into two parts in order to make the static RAM's footprint as square as possible. The program places a row decoder in the middle of the memory block.*

In addition to specifying the signal-connection requirements, you need to tell the program which processing technology you are using, the number of words in your static RAM, and the number of bits per word **(Fig 1).** After checking the validity of your inputs, the program splits the RAM into a right memory core, a row decoder, and a left memory core **(Fig 2).** This division brings the memory block's overall aspect ratio (ie, the ratio of the length to the width) close to one. Splitting the memory core also equalizes the amount of current drive that the column and row decoders respectively require.

Memory-core layout—right to left

The program first lays out the right core, which consists of pairs of memory-cell columns. The program then places a precharge cell at the top of each column, so the precharge transistor can supply its circuit. The program continues to place columns of memory cells until the RAM's size meets your specification. The static-RAM package repeats this procedure to complete the left memory core.

The next step in **Fig 1**'s flowchart shows that the program builds a word decoder (ie, the row decoder) in the center of the RAM. Placing the word decoder in the

center effectively distributes the current load on the last stage of the decoder. The number of words in the RAM determines the width and length of the row decoder.

Each row is automatically assigned a binary address, from 000 to 111. Because the RAM that the XRAM constructs uses only three address-input AND gates, there can be no more than eight addresses (binary 111). If your RAM contains more than 16 words, however, you can simply add more levels of decoding.

After the program has assigned all the addresses, it places metal contacts that connect either an address or an inverted-address signal to each AND gate's input. At the top of the last AND gate in the row decoder, the

Design package supervises program interaction

Fastrack is a supervisory software package that, together with the individual programs it controls, forms a semicustom-IC design system. To lay out the variable-size RAM portion of the IC, you must supply the system with artwork, pin-data, logic-simulation, and connectivity-certification files.

Usually, you start a Fastrack semicustom-IC design by using the Mimic logic simulator to verify your design. In its simulations, the Mimic program uses both functional and timing descriptions of all cells.

To help you simulate static memories, the expandable-RAM (XRAM) package provides a module that calculates internal propagation delays for the RAM. This module generates these delays by regarding the internal RAM structure as an RC tree and by recomputing the propagation delay for every expansion of the RAM. The module also includes the fan-out of the RAM's output drivers in the propagation-delay calculation.

Once you have verified your logic, you instruct the logic simulator to create a net list. You commence your memory-block layout by sending the logical net list to the Multi-Port 2-Dimensional (MP2D) automatic-placement and -routing program.

The MP2D package integrates memory blocks like the static-RAM block into your standard-cell design. The package defines the memory block as a rectangular area that has pins on at least one of its four sides; it then interfaces the block to the rest of the standard-cell IC. The program also lets you place such elements as I/O pads, alignment marks, and test transistors on your chip.

Although it imposes less stringent layout rules on the cells of the memory block than on a standard-cell layout, the program uses the same placement and routing procedures for memory blocks as for standard cells. The program can also distribute power lines throughout the IC. Because the layout package lets you define critical paths and optimize the routes for those paths, you can minimize parasitic capacitances.

Users must characterize pins

To connect the block to the rest of the IC, the layout system requires a pin-data file. This file contains a definition number for each part; a list of input and output pins and their respective Cartesian coordinates; flags that distinguish input pins from output pins; a name for each pin; and the height and width of the memory block.

The module that creates the RAM's artwork creates the pin-data file automatically. The MP2D program requires that all I/O pins fall on an integral multiple of a pin pitch (the sum of the width of the routing-metal line and the metal-to-metal spacing).

Although the program could force the dimensions of each cell in the sublibrary to be a multiple of the pin pitch, this approach would waste silicon real estate. Instead, the pin-data file-generating module takes the absolute X coordinate of each I/O pin and finds the nearest pin-pitch location. The router then connects the I/O pin to the rest of the memory block. This procedure eliminates the need to lay out subcells as a pin-pitch multiple.

When you've finished laying out your standard-cell IC, Fastrack calls the Concert (connectivity-certification) program. This program checks the electrical connectivity of the circuit, evaluates the parasitic capacitances, and generates a net list, which you can compare with the logic simulator's net list to see if you have introduced any errors.

Because the software implements an algorithm that views the RAM layout as a 2-D geometric process, the program can handle all processing technologies.

layout package completes the row decoder by placing an address-inverting/noninverting buffer cell.

Following the completion of the decoder, the program adds a 2:1 multiplexer (a column switch), a sense amplifier, and a data-I/O buffer to the bottom of each pair of memory-core columns. The column switch selects which of its two columns the associated sense amplifier will service at a given time. To complete the layout, the package places write-enable and chip-select buffers (the control logic) and a column decoder in the empty space below the row decoder.

Program handles any technology

Because the software implements an algorithm that views the RAM memory-block layout as a 2-D geometric process, the program can handle all processing technologies. For each technology, you must supply a cell library and one technology file. The cell library contains approximately 12 cells. The technology file is a list of the cells' internal dimensions, including such data as the height and width of cells and the absolute coordinates of AND-gate inputs relative to the fiducial coordinates of the AND cells.

Once you have obtained a RAM sublibrary for the technology you are using, you must align the subcells in your layout so that all signal buses and power supplies line up. This placement is necessary because the router doesn't let you interactively edit routing paths inside the memory block.

The static-RAM design system lets you lay out cells that can contain any number of transistors. In addition, your RAM can use bidirectional I/O ports or separate inputs and outputs. What's more, the sense amplifier can be a differential amplifier or a simple inverter. You must, of course, use only circuits that are included in the XRAM package.

Expanding the RAM

Once you have outlined your static RAM, you can expand the number of bits per word in increments of one bit per word and expand the word size in 4-word increments. The minimum RAM size is four words (at four bits per word).

If you don't intend that your RAM use words of the form 2^N—you expect, for example, to use 30 of 32 bits—you won't need to access every memory cell. This discrepancy should occasion no worry, however: If you don't route any connections to unused cells, an erroneous address won't be able to access those cells. You also might not want to use some of the address lines that connect to the inputs of the decoder's AND gates. In this event, the program automatically connects unused AND-gate inputs to the supply voltage and designates these inputs as inaccessible.

Factors such as the speed of signal propagation in the RAM and the relation of the memory block's size to the overall size of your IC limit the maximum size of the RAM. The upper limit on the RAM's size is 1k bits; the maximum word size is 32 bits per word.

Using the XRAM package, you can construct a 1k-bit static RAM, like the 64-word×16-bit RAM shown in **Fig 3,** which specs 60-nsec read and write cycle times. The operating current of the 1k-bit RAM is 350 μA per word bit; the standby current is 1.5 μA per bit. **EDN**

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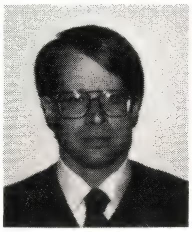
1. Stebnisky, M W, M J McGinnis, J C Werbickas, R N Putatunda, and A Feller, "Fully automatic PLA subchip generator: A logical design interface," GOMAC Conference Proceedings, 1982.

Authors' biographies

Abed Mougharbel is an associate member of the technical staff at RCA's Solid State Division (Somerville, NJ), where he specializes in software development and system integration for the semicustom-design group. In 1983, he received simultaneous bachelor's degrees from Columbia University and Hamilton College in electrical engineering and mathematics, respectively. Abed enjoys fishing, scuba diving, listening to music, and drawing.



Subsequent to his participation in writing this article, Tom Housten moved from RCA's Solid State Division to Siemens Research Laboratories (Princeton, NJ), where he is an IC design engineer. He received a BSEE from the New Jersey Institute of Technology in 1974. In his free time, Tom enjoys backpacking, skiing, and listening to music.

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CIRCLE NO 153

Parallel processing suits real-time applications

Many real-time applications are better served by a parallel-processing computer architecture than by a general-purpose single-CPU system. By carefully dividing software tasks and providing efficient communications, you can implement a parallel-processing system that's powerful enough to handle complex real-time tasks.

Marco Salzwedel, *Consultant* and
Friedhelm Baisch, *DFVLR*

The Spacemed computer *includes global-memory, CPU, and I/O-control boards in a VME Bus format. The computer acquires data, performs data-processing tasks, and displays the results.*

For the high-speed data-acquisition and -processing capabilities required by real-time applications, consider implementing a parallel-processing system. By constructing the computer from a group of parallel computing elements that share data-processing tasks, and by furnishing efficient communication paths between the computing elements, you can increase the system's performance.

To develop a parallel-processing system, you'll have to pay careful attention to your computer's architecture. You'll need an efficient memory organization, as well as a careful division of software tasks. You'll also have to consider system-control issues to minimize administrative overhead and to optimize system efficiency. Several simple formulas let you approximate relative performance and calculate the efficiency of a parallel-processing system.

Such a computer system is being developed for the Aerospace Medicine Institute of the West German Space Agency, DFVLR. The system, called Spacemed, monitors and processes the electrocardiogram (EKG) and impedance-cardiogram (IKG) waveforms obtained

Parallel-processing systems require efficient memory organization and careful division of software tasks.

from astronauts during space shuttle missions, and it processes data at speeds that range from ×1 to as high as ×10 real-time rates. The computer thus requires only 2.4 hours to process EKG and IKG data acquired over 24 hours. The real-time sampling rates range from 1 kHz to as high as 10 kHz.

The Spacemed computer is meant not for general-purpose computations but for real-time data-acquisition, analysis, and control applications. However, the hardware and software provide flexibility, so programmers can reconfigure the computer for new or modified real-time medical data-processing tasks. In addition, Spacemed serves as a model for parallel-processing systems dedicated to real-time tasks.

Share tasks among CPUs

Unlike parallel-processing computer systems, conventional computer systems provide one central-processing unit (CPU) that processes one stream of data and instructions. Such computers are often too slow for real-time needs. You can increase computer power through parallel processing, designing the main computer from a group of parallel computing elements that share data-processing tasks. Nevertheless, parallel operations raise two basic problems: You must efficiently divide the processing problem into parallel tasks, and you must furnish communication paths so the tasks can communicate.

Dividing your tasks efficiently is no trivial matter because parallel operations often depend on one another. For example, in the equation $E=(A\times B)+(C\times D)$, parallel processors perform the two multiplication operations in parallel. The main computer, however, must have both multiplication results before it can perform the addition. If one of the multiplication operations is slow, the computer remains idle while it waits for the result. Parallel processors thus require an efficient communication structure as well as careful task coordination.

Unlike tightly coupled parallel-processing systems, the Spacemed computer relies on a data-flow architecture. In tightly coupled computer systems, tasks are generally of equal length, and tasks transfer information to each other through a set of stack registers. Before running the next set of tasks, the computer must have all of the data from the previous tasks. As a result, the computer can remain idle, or deadlocked, for lack of information until the slowest task finishes.

To avoid the data-deadlock problem, the Spacemed computer relies on a communication structure that transfers information between modules through large-capacity circular buffers. The modules are self-sufficient; that is, they contain all the information they need to process data and transfer control to and from the local host's control program. Rather than transfer data one value at a time through a stack register, the modules access the circular buffers, which can contain many values. By staying somewhat behind a backlog of data, modules always have information to process. Each module monitors the amount of data available in its buffer and varies its requests for processing time accordingly. For example, as a buffer approaches overflow, the module requests processing time more frequently than it would if the buffer was almost empty.

The communication channel must be fast enough to store results and supply data to parallel processors without creating bus bottlenecks. Communication-channel architecture varies with the parallel-processing architecture you use; generally, though, you increase communication-channel complexity when you add processors.

When you plan the structure of a parallel-processor computer system, you'll have to consider two major design issues: system control and distribution of code and data. System control involves keeping the computer's administrative overhead tasks at a minimum. You must also consider how to have your main computer distribute tasks to the parallel processors. You might, for example, choose to assign tasks dynamically: The computer continuously analyzes the program and divides its tasks among the available processors. By applying the dynamic-assignment method to most serial programs, you can balance the workload among available processors. However, the task-assignment and program-transfer operations require extra overhead time, reducing the amount of time left to process information.

As an alternative to assigning tasks dynamically, consider assigning tasks to processors before the computer starts processing data. Once assigned, a task operates within a single processor, and the computer no longer requires extra time to analyze a program and reassign tasks to available processors. Nonetheless, you can't apply static task assignments to a program unless the program has a data-flow structure.

Consider storage tradeoffs

Also, because tradeoffs exist between information- and program-storage techniques, consider where to store data and program code. The system provides two

types of memory: global memory that all processors access over the system's bus, and local memory that's dedicated to each processor. For example, such data as the real-time clock's time must be accessible to all parallel processors, so you save it in global memory. On the other hand, specific program code for one parallel processor is useful only to that particular processor. By saving information in the system computer's global memory, the system needn't maintain copies for each parallel processor. But, because all processors can access the data in global memory, any one of those processors can improperly modify the information that the others depend on.

You can store each parallel processor's program code in the system computer's global memory, from which each processor obtains its code. Such global data transfers increase the bus's overhead processing time, thus reducing the time the bus has for other tasks. To reduce bus overhead, construct parallel-processor boards so that each contains a local memory for program storage. After loading the program code into the parallel processor for a particular task, the computer system's global bus is free for other uses.

Parallel-processing computer systems fall into two general categories: single-instruction, multiple-data stream (SIMD) or multiple-instruction, multiple-data stream (MIMD). SIMD processors perform the same operation on several pieces of data at the same time, but only one instruction stream controls the data-processing tasks. For example, you can process a TV

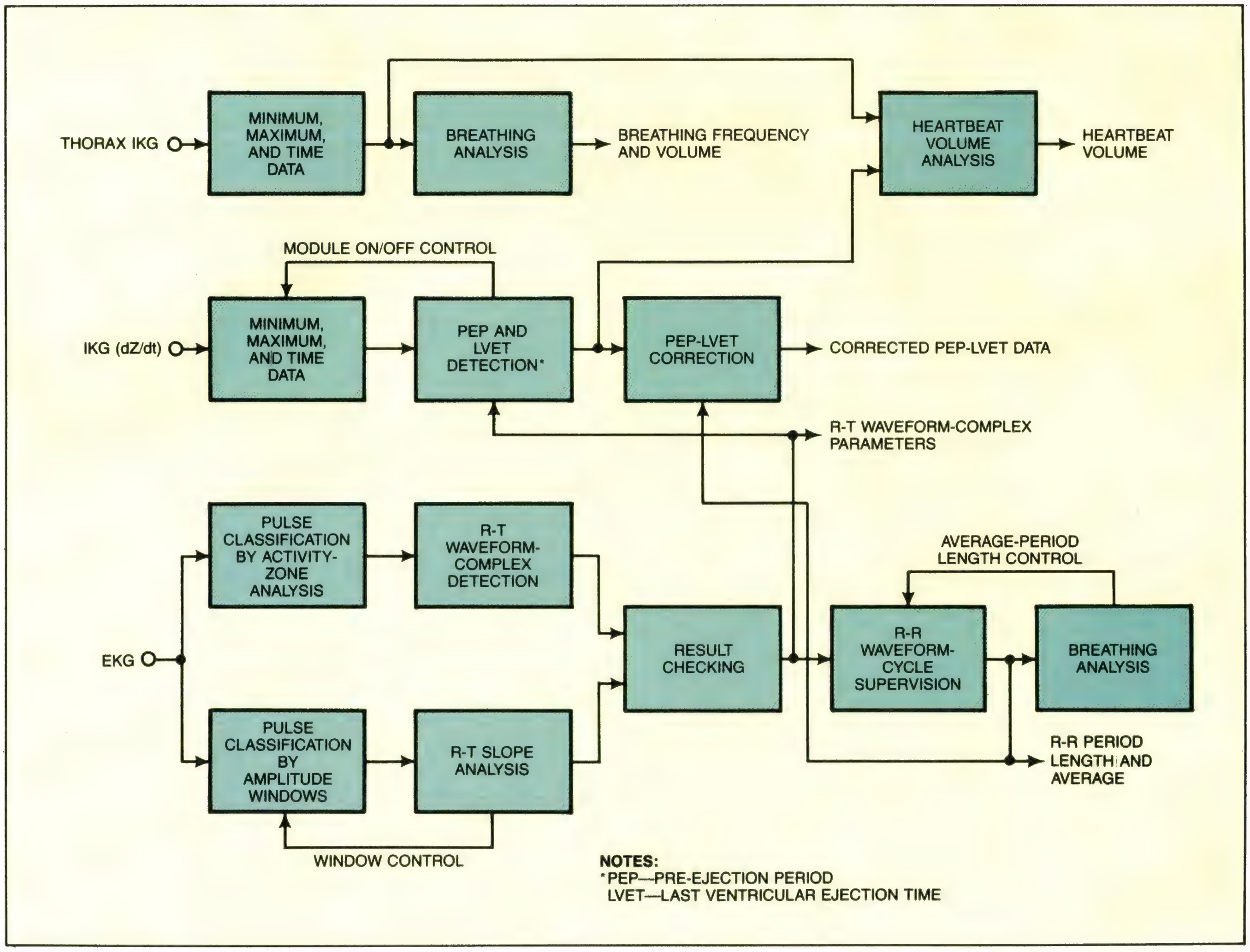

Fig 1—Spacemed software *includes independent task modules that acquire and process physiological information obtained during flights of the space shuttle.*

Parallel processing—constructing the main computer from a group of parallel computing elements that share tasks—lets you increase computer power.

image by dividing the image into small groups of pixels and assigning a group to each processor. A common instruction stream controls all the processors in parallel, thus manipulating the data faster than one computer that operates on one pixel at a time.

In MIMD systems, on the other hand, several processors run asynchronously and independently, and each processor has its own instruction stream. MIMD systems are relatively complex, requiring an extensive support structure that includes control and interface circuits, as well as a control program and RAM for program and data storage for each processor. MIMD systems adapt well to tasks that require simultaneous but different operations—for example, motor control and data acquisition.

The Spacemed computer relies on the MIMD structure. When the computer starts, the system selects one processor as the system host. The system host's responsibilities include task distribution, system timing, system supervision, and communication handling. The remaining processors become local hosts, which are responsible for the tasks the system host assigns them. To provide fault tolerance, the processors continually check each other. Should a processor fail, the system starts a reconfiguration cycle, which selects a new system host or redistributes a failed local host's tasks, depending on which processor failed. Thus, a processor failure may degrade the system's performance, but it doesn't completely shut the system down.

A complete data-acquisition and -monitoring program is a set of functional modules that performs small but complete functions such as peak-height analysis or data-format conversion **(Fig 1)**. The system host assigns modules to each local host and, in turn, the local

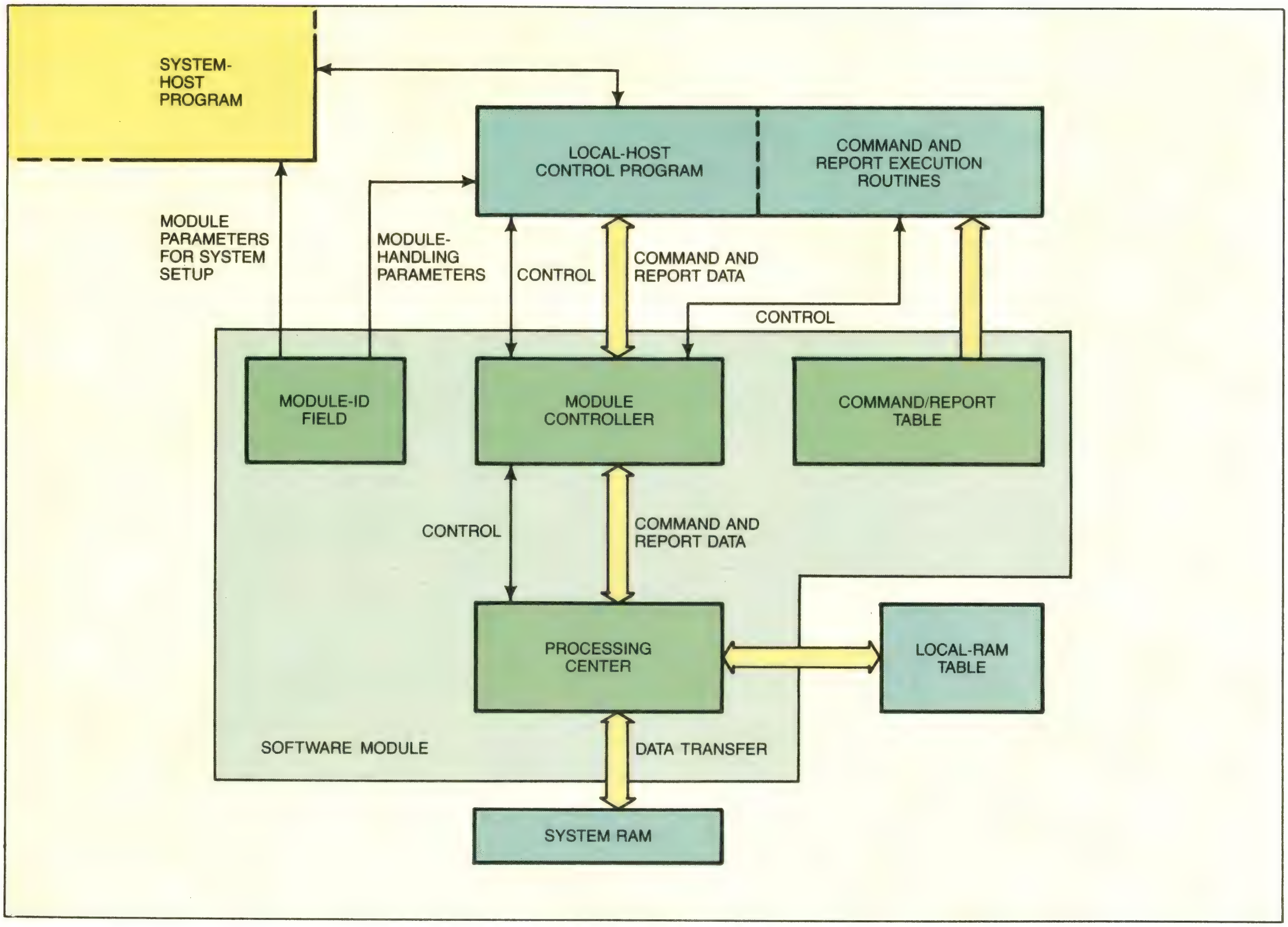

Fig 2—A typical parallel-processing software module *includes a module controller that provides the interface with the local computer. The processing center performs the I/O or data-processing tasks.*

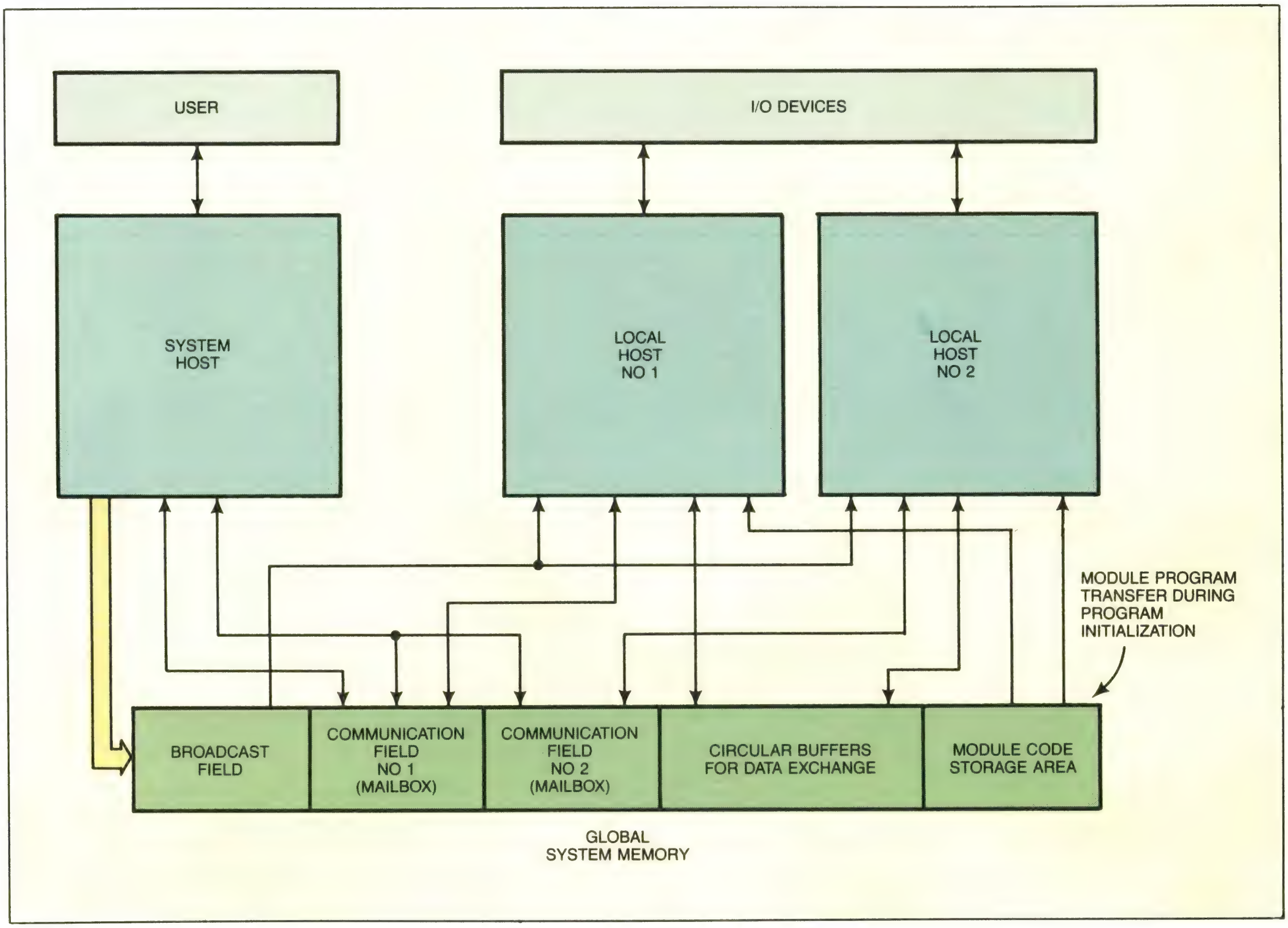

Fig 3—The global memory structure *contains circular buffers for each module's data. The memory also provides communication fields for each local host and a broadcast field for messages going to all local hosts.*

hosts obtain their program code from the system's global memory. Each of the parallel-processor modules is generally independent, and modules don't share subroutines or code segments. The self-sufficient modules isolate programming errors, assist in program debugging, and allow for fault-tolerant software design.

The processing-center software is the heart of the module: It contains the program that performs the module's I/O or data-processing tasks. Besides software, each module contains module-control and processing-center hardware **(Fig 2)**. The module-control hardware performs housekeeping tasks and passes commands and responses between the local host's control program and the processing-center hardware.

In addition, each module contains a module-ID field and a command-report parameter table in its software. The module-ID field holds information that tells the system computer what resources are required for the module; it contains an ID number, module length, the number of available I/O channels, processing-time requirements, data-flow speeds, etc.

Standard formats ease module development

The command-report parameter table contains command and parameter strings that define reports and commands that travel between the module and the local host. Typical strings include information for such conditions as data overrun and command-format error. Standard command and report formats simplify the tasks of developing, testing, and using individual task-oriented software modules.

Each module also includes instructions that transfer information between two RAM structures serving dif-

Dividing tasks efficiently is no trivial matter because parallel operations often depend on one another.

ferent purposes. The circular buffers—based in the system's global memory—provide a read and a write pointer for a module. They also supply the only data-transfer path between the modules.

The local host and the module exchange commands through a line buffer in the local host's RAM. The host always transfers commands or reports to the module when the module starts its operation. After the module completes its task, it transmits commands or reports to the local host. The local host also provides a pointer that locates a block of RAM for each module. The module accesses any location in the RAM, but its addresses are relative to the pointer. Typically, modules use the local RAM to store intermediate data, counter values, and other information not sent to system memory.

The system's global memory contains three data structures that handle information-transfer operations between the system's components (**Fig 3**): global circular buffers, addressed-data packet channels (mailboxes), and a broadcast-communication field for messages for the entire system.

The system host assigns each module its own circular buffers for numeric results, data from input devices, or data for other modules. Although only one module puts data in an assigned circular buffer, several modules can read the buffer's contents. The data in a circular buffer contains no addresses or pointers. Instead, each buffer has an associated storage block that contains descriptive information about the size of the buffer and the location of the current data block. The circular buffers provide high-capacity, high-speed storage that requires little control by the system computer. Buffers vary in size from 1k byte to as much as several million bytes.

To transfer I/O-device information, module status, and module commands, the global memory includes a mailbox for each local host. Each mailbox contains two circular buffers that contain small blocks (packets) of information. Each packet includes header and address information that identifies the receiver, a module, a host, an I/O device, or the user. The system host controls the distribution of packets to the proper mailboxes.

Broadcast field holds time data

The global memory also contains a broadcast-communication field that transfers information to all local hosts. The system host provides a system-reference time from a real-time clock in the broadcast-communication field. The current time is thus always available to the local hosts.

Communication between all the computers and the system computer's global memory determines the efficiency of the shared-memory parallel-processing system. In theory, processing power (throughput) is proportional to the number of parallel processors in the system. Practical limitations on the speed of the system's bus and the memory's response time set an upper limit on efficiency, however. As you add processors to a parallel-processing system, you'll eventually reach a peak in efficiency. Once you've reached this peak, adding more processors may actually decrease efficiency: The added processors spend most of their time vying for bus control. The parallel processors thus wait to access memory when they should be processing data.

Because response times vary from task to task, you'll have to determine the maximum acceptable response time for your application. In such processes as process-temperature monitoring, real-time response may be several seconds. For real-time response to heartbeat signals, the longest response time is 1000 μsec.

Under conditions when no backlog of data awaits processing, and when the module-switching algorithm calls each module with the same frequency, you can approximate the maximum response time (MRT) with the following equation:

$$MRT=P_1+P_2\ldots+P_n+(S\times n/T).$$

MRT is expressed in system-time units (STUs). The STU is an artificial reference period that relates to the sampling rate you use to measure an external signal. In the Spacemed system, real-time data acquisition occurs at 1-msec intervals, so T is 1000 μsec. The P_n values represent the periods (in STUs) that the local computer allots to each module. You must supply a P_n value for each of the n modules in a task. Switching between modules also requires processing time; the S term represents module-switching time in microseconds.

Calculate processing efficiency

You can also calculate the processing efficiency of your computer system, ie, the amount of time the computer spends processing data vs its total processing time. As administrative time increases, your computer's efficiency decreases according to the following expression:

$$E=1-[(n\times S)/(MRT\times T)].$$

The resulting efficiency value (E) is between 0 and 1;

1 represents the highest efficiency (all tasks processed on time). A negative result indicates an impossible situation: Housekeeping tasks overwhelm the processor and no data is processed.

A computer's efficiency also depends on how you divide tasks among the parallel processors. In general, you'll assign at least one task to each processor (it usually makes no sense to leave a processor idle). Nevertheless, dividing a task into too many modules can slow processing. As you increase the number of modules and make them simpler, you force the computer to execute more data- and instruction-transfer operations. The result is diminishing returns because housekeeping tasks consume more of the computer's processing time. **EDN**

Authors' biographies

Marco Salzwedel is a consultant who develops real-time computer hardware and software for military, R&D, and industrial applications. Based in San Francisco, CA, since 1984, Marco works on the Spacemed project. He enjoys travel, science, and amateur radio as leisure activities.

Friedhelm Baisch heads the space-physiology and medical branch of the West German Space Agency, DFVLR, where he has worked since 1980. He is responsible for the medical aspects of Spacemed and for overall project management. He received his doctor of medicine degree from the Free University of Berlin in 1978. His hobbies include reading and classical music.

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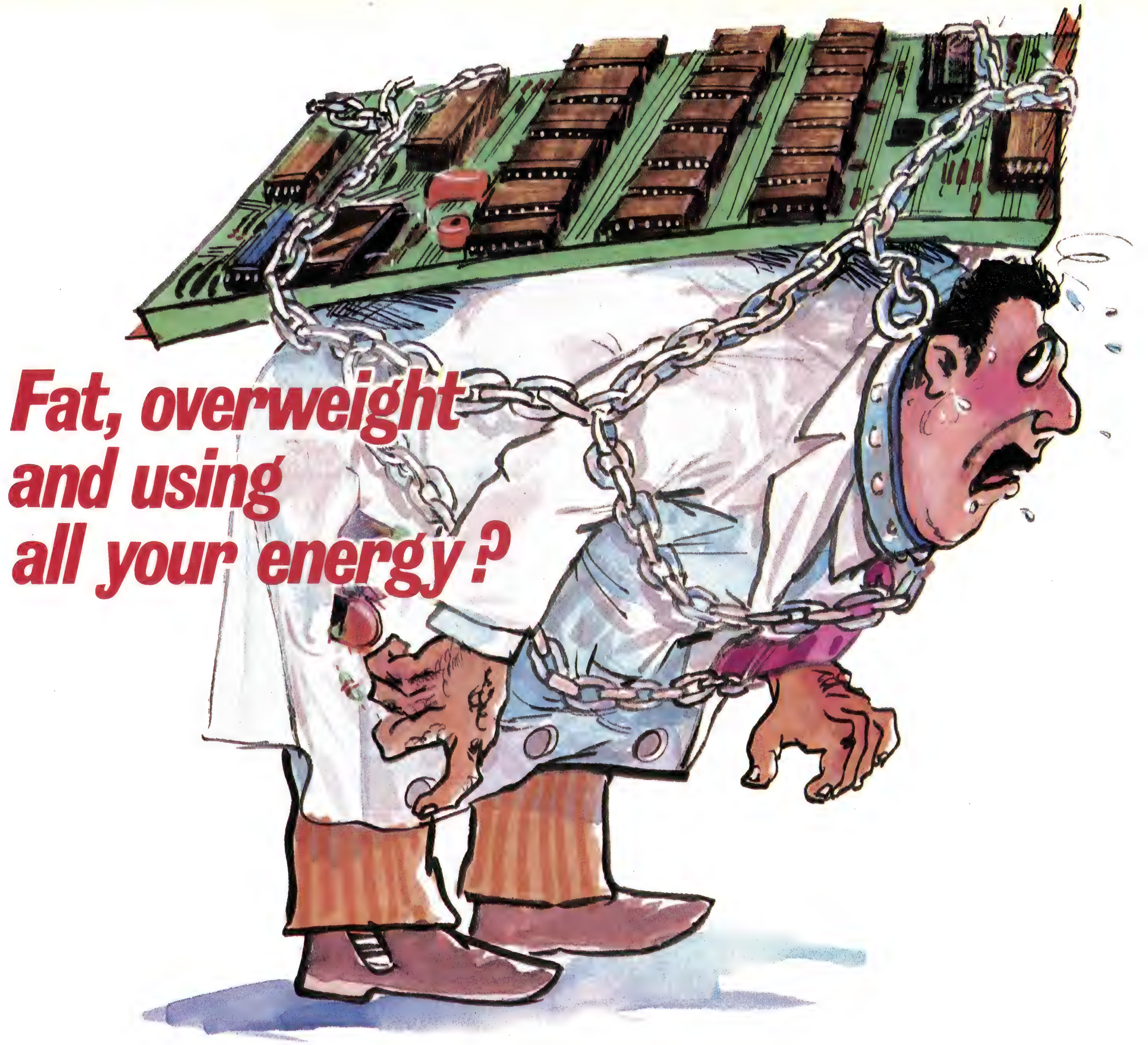

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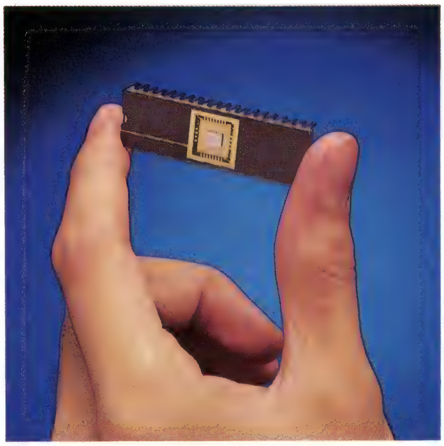

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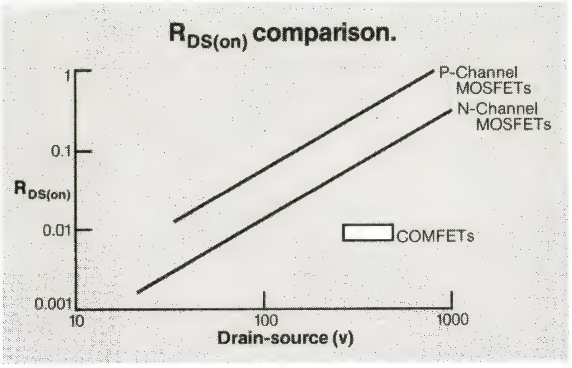

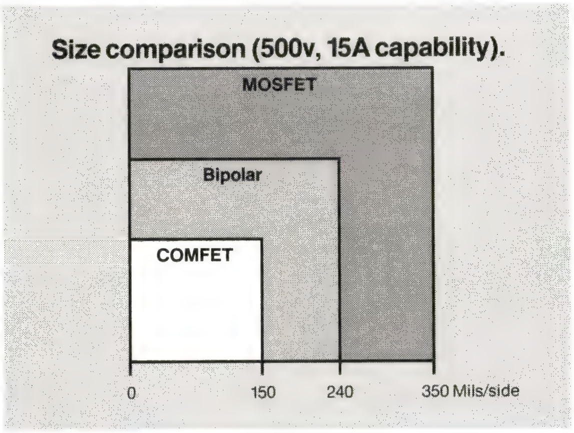

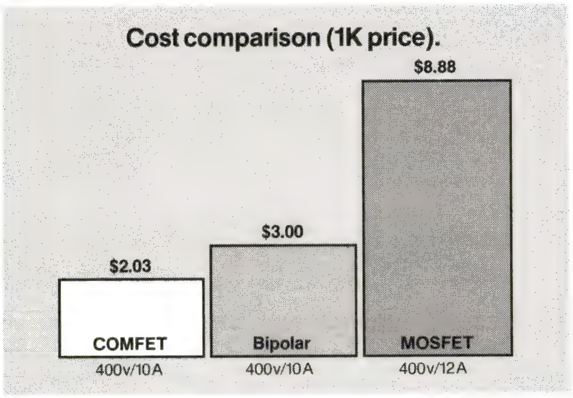

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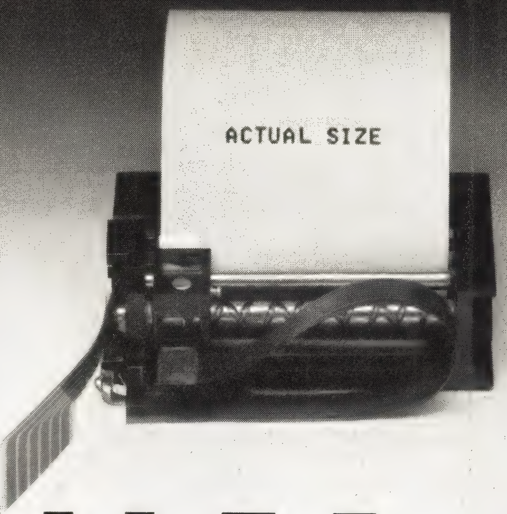

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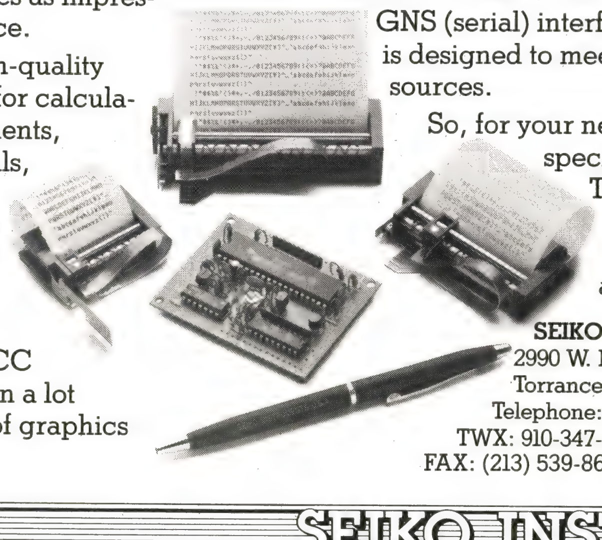

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Minimize hardware for Z80 start-up routine

Paul Alesu
Icsite, Bucharest, Romania

A Z80 µP system can implement the **(Fig 1)** start-up function with an 8212 input port **(Fig 2),** thereby using memory space in place of an additional timer and interrupting hardware. The timer-clock period must equal six system-clock periods.

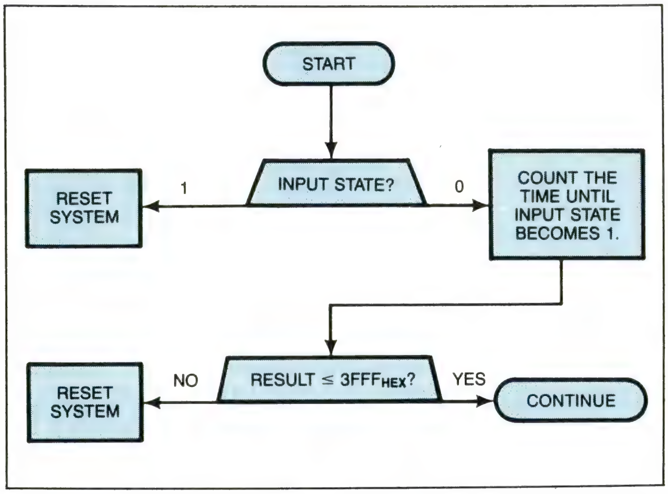

Fig 1—Normally, an input port, timer, *and other hardware are required to implement this start-up sequence in a Z80 system.*

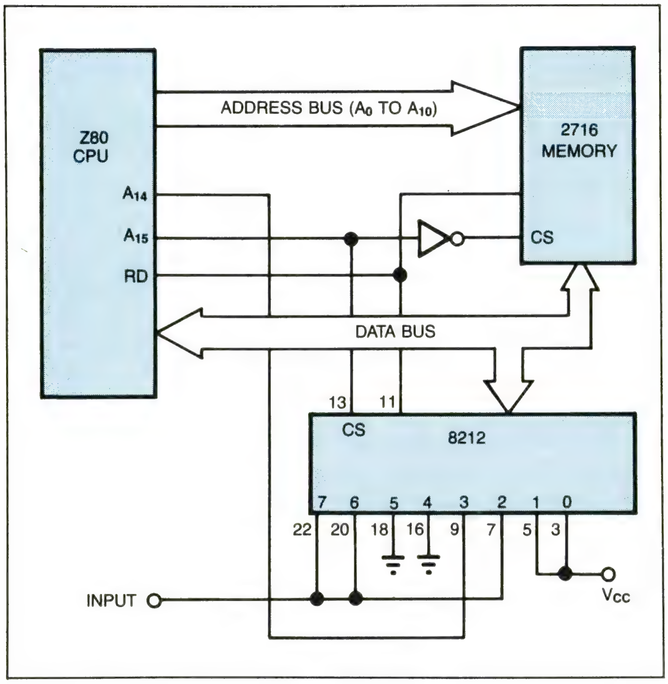

Fig 2—An 8212 input port and some memory *implement the* ***Fig 1*** *start-up sequence in this Z80 system.*

TABLE 1—INSTRUCTIONS PASSED FROM 8212 PORT TO CPU

A15	A14	INPUT	1-BYTE INSTRUCTION	
1	0	0	03	INC BC
	0	1	C7	RST 0
	1	0	0B	DEC BC
	1	1	CF	RST 8
0	8212 INPUT PORT NOT SELECTED			

TABLE 2—ALTERNATIVE CODE SEQUENCES EXECUTED BY THE Z80

```
1ST SEQUENCE:
00F1  01 FFFE  1D BC, 0FFFEH    ;BC REGISTER SETTING
00F4  C3 BFFF  JP 0BFFFH        ;JUMP
BFFF  C7       RST 0            ;HIGH STATE INPUT AT THIS
                                ;MOMENT RESTARTS THE SYSTEM

2ND SEQUENCE:
00F1  01 FFFE  1D BC, 0FFFEH    ;BC REGISTER SETTING
00F4  C3 BFFF  JP 0BFFFH        ;JUMP
BFFF  03       INC BC
C000  0B       DEC BC           ;LOW STATE INPUT ENABLES
C001  0B       DEC BC           ;COUNTING
C002  0B       DEC BC           ;
               .........
C215  0B       DEC BC           ;
C216  0B       DEC BC           ;
C217  CF       RST 8            ;HIGH STATE INPUT AT THIS
                                ;MOMENT ENABLES JUMP TO
                                ;A SUBROUTINE

3RD SEQUENCE:
00F1  01 FFFE  1D BC, 0FFFEH    ;BC REGISTER SETTING
00F4  C3 BFFF  JP 0BFFFH        ;JUMP
BFFF  03       INC BC           ;
C000  0B       DEC BC           ;LOW STATE INPUT ENABLES
C001  0B       DEC BC           ;COUNTING
C002  0B       DEC BC           ;
               .........
FFFD  0B       DEC BC           ;
FFFE  0B       DEC BC           ;
FFFF  0B       DEC BC           ;
0000  --       ---              ;LACK OF INPUT SIGNAL LEADS
                                ;TO SYSTEM RESET
```

When selected, the 8212 port passes a 1-byte instruction to the CPU **(Table 1).** As a result, the system runs one of the three code sequences in **Table 2,** depending on the moment at which the input signal goes high.

EDN

To Vote For This Design, Circle No 750

C function calls the IBM PC I/O system

Jeffrey Anthony
Corby Industries Inc, Whitehall, PA

For use with IBM PC and compatible computers, the assembly-language subroutine of **Listing 1** allows you to call the computer's basic I/O system (BIOS) from the high-level compiled C language. (Although many compilers support calls to the host computer's operating system, few allow access to the host's BIOS.) The C-callable function "Bios" is written for the Whitesmith C compiler, but it can be used with other production C compilers after slight modifications.

Bios invokes the BIOS call specified by its parameter call number (callnum) by causing a software interrupt of the same number. Assignment statements at lines 19 and 20 allow you to port the Bios function to many C compilers. The Base variable is the number of bytes between where the stack pointer (sp) and the pointer to the first (zeroth) parameter are stored. Offset (line 19) is the stride of subsequent contiguous pointers. Lines 28 and 29 save the frame pointer bp (the base pointer) on the stack, and then move sp to bp for use in subsequent memory manipulations.

Lines 31 through 38 load the Bios function parame-

LISTING 1

```
                bios - call IBM PC bios function

                SYNOPSIS:
                        int bios(callnum, ax, bx, cx, dx)
                                unsigned callnum
                                unsigned *ax, *bx, *cx, *dx




017:    .public _bios
018:    _bios:
019:            OFFSET = 4                              / compiler dependant data
020:            SIZE = 2
021:
022:            p0 = OFFSET                             / parameter locations
023:            p1 = p0 + SIZE
024:            p2 = p1 + SIZE
025:            p3 = p2 + SIZE
026:            p4 = p3 + SIZE
027:
028:            push    bp                              / save frame pointer
029:            mov     bp,sp                           / set bp to base address of
030:                                                    / parameter list
031:            mov     si,[bp][p1]                     / move params to registers
032:            mov     ax,[si]
033:            mov     si,[bp][p2]
034:            mov     bx,[si]
035:            mov     si,[bp][p3]
036:            mov     cx,[si]
037:            mov     si,[bp][p4]
038:            mov     dx,[si]
039:            mov     si,[bp][p0]                     / get interupt number
040:
041:            cmp     si,0x10                         / call designated interrupt
042:            je      video
043:            cmp     si,0x11
044:            je      hrdtst
045:            cmp     si,0x12
```

```
                 je      mem
                 cmp     si,0x13
                 je      diskio
                 cmp     si,0x14
                 je      comm
                 cmp     si,0x15
                 je      cassio
                 cmp     si,0x16
                 je      keyio
                 cmp     si,0x17
                 je      prtio
                 cmp     si,0x18
                 je      cbasic
                 cmp     si,0x19
                 je      boot
                 cmp     si,0x1a
                 je      time
                 cmp     si,0x1b
                 je      keybrk
                 cmp     si,0x1c
                 je      tick
                 cmp     si,0x1d
                 je      vidint
                 cmp     si,0x1e
                 je      dskint
                 cmp     si,0x1f
                 je      chrint
                 mov     ax,0xffff              / set return value to error
                 jmp     quit
        video:   int     0x10                   / video
                 jmp     exit
        hrdtst:  int     0x11                   / hardware test
                 jmp     exit
        mem:     int     0x12                   / mem size
                 jmp     exit
        diskio:  int     0x13                   / disk I/O
                 jmp     exit
        comm:    int     0x14                   / RS-232 I/O
                 jmp     exit
        cassio:  int     0x15                   / cassette I/O
                 jmp     exit
        keyio:   int     0x16                   / keyboard I/O
                 jmp     exit
        prtio:   int     0x17                   / printer I/O
                 jmp     exit
        cbasic:  int     0x18                   / cassette BASIC
                 jmp     exit
        boot:    int     0x19                   / bootstrap
                 jmp     exit
        time:    int     0x1a                   / system time
                 jmp     exit
        keybrk:  int     0x1b                   / keyboard break
                 jmp     exit
        tick:    int     0x1c                   / timer tick
                 jmp     exit
        vidint:  int     0x1d                   / video initialization
                 jmp     exit
        dskint:  int     0x1e                   / disk initialization
                 jmp     exit
        chrint:  int     0x1f                   / character initialization
                 jmp     exit
        exit:    mov     bp,sp                  / move registers to params
```

Continued on pg 230

```
111:                mov     si,[bp][p1]
112:                mov     [si],ax
113:                mov     si,[bp][p2]
114:                mov     [si],bx
115:                mov     si,[bp][p3]
116:                mov     [si],cx
117:                mov     si,[bp][p4]
118:                mov     [si],dx
119:                mov     ax,0x0000                / set return value to 0
120:
121:        quit:   pop bp                           / restore frame pointer
122:                ret
123:                .data
```

ters into their associated registers. Line 39 loads the BIOS call number into the string index (si) register for analysis by lines 41 through 72, which transfer control to the designated software interrupt in lines 77 through 108. Lines 74 and 75 set the return value to −1 if an invalid BIOS call number is passed to the function.

The function takes as parameters the values loaded into the 8086 or 8088 µP's ax, bx, cx, and dx registers before the BIOS call. After return from the designated interrupt, control is passed to lines 110 through 118, which store the register contents in the associated parameter locations—modifying the parameter values as a side effect of executing the function. Line 119 sets the return value to 0 to indicate that a valid BIOS call number was passed to the function and executed. Finally, lines 121 and 122 restore the frame pointer to the bp register and return control to the calling C function.

Assembly of the Bios function must produce a relocatable image suitable for use with the host operating system's linker/loader. After being declared externally, Bios can be called as a C function. **EDN**

To Vote For This Design, Circle No 748

CRT-brightness control is opto-isolated

Michael Karas
O A Systems Inc, Culver City, CA

CRTs require various ranges and polarities for the brightness-control voltage input. The **Fig 1** circuit meets many of these requirements by providing a digitally controlled linear voltage as high as 200V in either polarity. Further, an optocoupler (IC_3) isolates the brightness circuits from the CRT to avoid the electrical noise associated with a flyback transformer in the CRT's high-voltage power supply.

You load brightness data in the form of 8-bit digital words from the system's data bus to the double-buffered D/A converter. A corresponding analog voltage between 0 and −5V appears at the output of op amp IC_{2A}.

Op amps IC_{2C} and IC_{2D} form a triangle-wave generator whose frequency is determined by R_2 and C_1. This waveform is shifted negative by R_5 and R_6 for comparison with the control voltage from IC_{2A}. Op amp IC_{2B} operates in open-loop fashion (as a comparator) to produce a pulse output of constant repetition rate and a pulse width proportional to the control voltage.

Positive pulses overdrive the optocoupler to eliminate the effect of temperature on the coupler's forward current-transfer ratio. These pulses pass through the optical barrier and enter the output integrator, which regenerates the control voltage for presentation to the CRT. Negative pulses at the optocoupler are clamped by diode D_1 to protect the coupler from reverse bias.

Diodes D_2 through D_5 form a bridge that ensures a positive voltage across the R_9-R_{10} divider for either polarity of the voltage you connect to the TOP and BOT control connections. Consequently, the ARM terminal's voltage makes a linear swing between the voltage levels applied to the TOP and BOT terminals.

The component values in **Fig 1** allow you to replace a nominal 100-kΩ brightness control, using a TOP-to-BOT bias voltage as high as 200V. To replace a lower-resistance control, you may have to increase the value

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1000-2000 MHz	25 dB min.
2000-2500 MHz	20 dB min.
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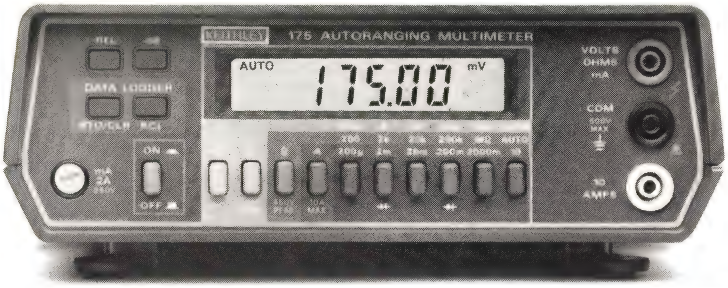

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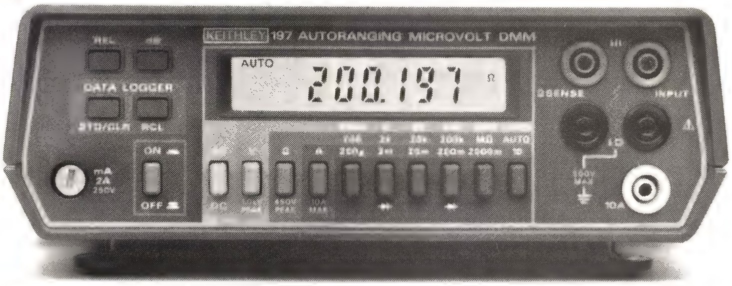

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of C_2 or increase the triangle-wave frequency (by lowering the value of R_2), to avoid unacceptable ripple at the collector of Q_1.

Voltage dividers R_3-R_4 and R_5-R_6 set the voltage levels of the triangle-waveform tips appearing at the output of IC_{2B}, which in turn set the maximum and minimum brightness levels. You adjust these resistor values to make the desired limits for brightness correspond to the minimum and maximum inputs to the D/A converter (00_{HEX} and FF_{HEX}). **EDN**

To Vote For This Design, Circle No 749

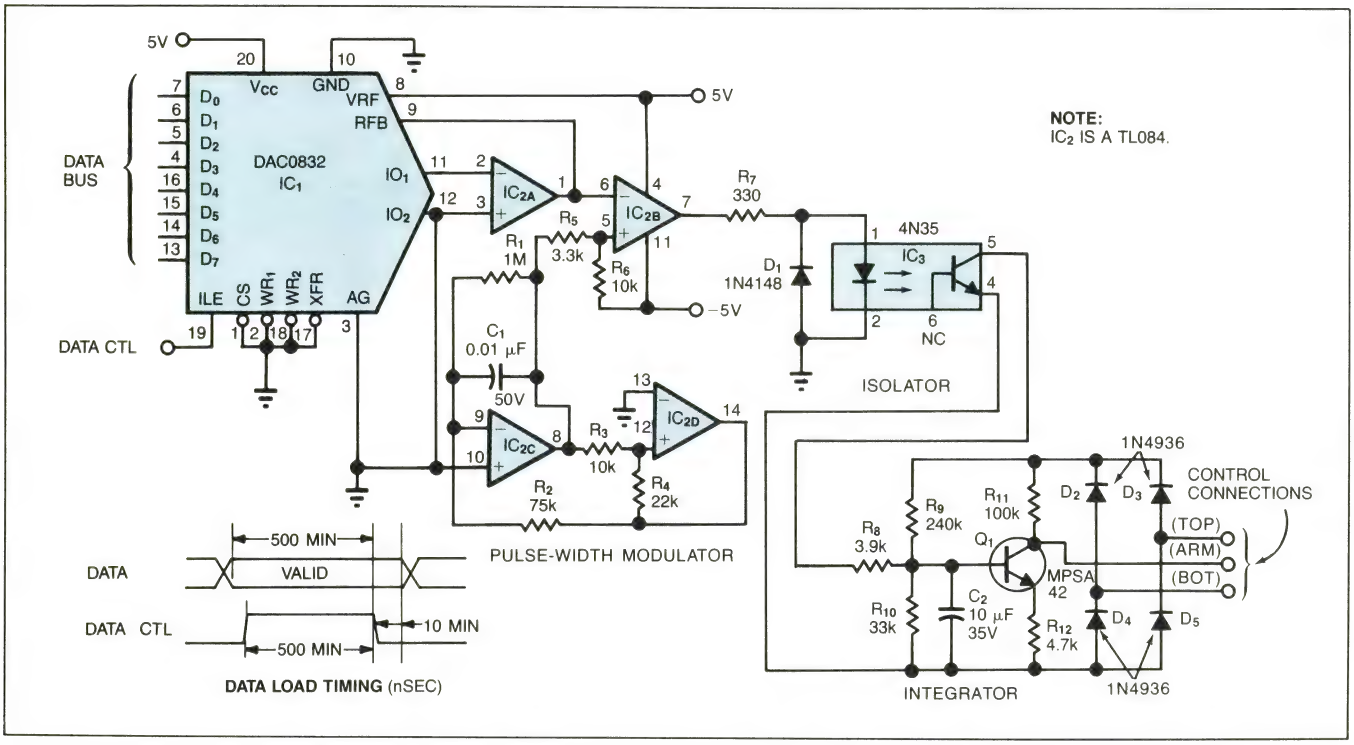


*Fig 1—**Digital control for CRT brightness** provides a control voltage (ARM) as high as 200V with polarity determined by the bias voltage you connect between the TOP and BOT terminals. Optocoupler IC_3 provides ground isolation to avoid noise from the CRT's high-voltage circuits.*

Multiplier serves as a high-speed switch

Barrie Gilbert
Analog Devices, Forest Grove, OR
and Charles Kitchin
Analog Devices, Wilmington, MA

By combining a \$10 analog multiplier with a \$2 wideband op amp (**Fig 1**), you can make a high-speed spst switch that has a 50-nsec response and a bandwidth that exceeds 30 MHz. The switch uses both channels of an AD539 multiplier to provide two features: the option of inverting or noninverting inputs, and the elimination of the switching pedestal caused by step changes in output current as the multiplier is gated on or off.

Gain is approximately 1 (0 when off). The output can drive ±1V into a 75Ω load or ±2V into a 150Ω load. An output-offset adjustment is optional.

The **Fig 2** waveforms were taken across a 75Ω termination. In **Fig 2a**, the output response to a 0 to 1V, 1-MHz sine wave shows the switching completed in about 50 nsec. Feedthrough of the control signal is minimal; feedthrough of the sine-wave signal (off isolation) is approximately −55 dB, determined largely by parasitics in the board layout. In **Fig 2b**, response to a 0 to 1V pulse in the signal channel shows a rise time of

less than 10 nsec (control input held at 0V). Response from the inverting input is similar.

Differential gain (less than 0.05 dB) and differential phase (less than 0.5° at 3.58 MHz) are compatible with video applications. Output noise with a 75Ω load is 200 μV typ in a 0- to 5-MHz bandwidth, or approximately 100 nV/√Hz. The noise spectral density is essentially flat to 40 MHz. **EDN**

To Vote For This Design, Circle No 746

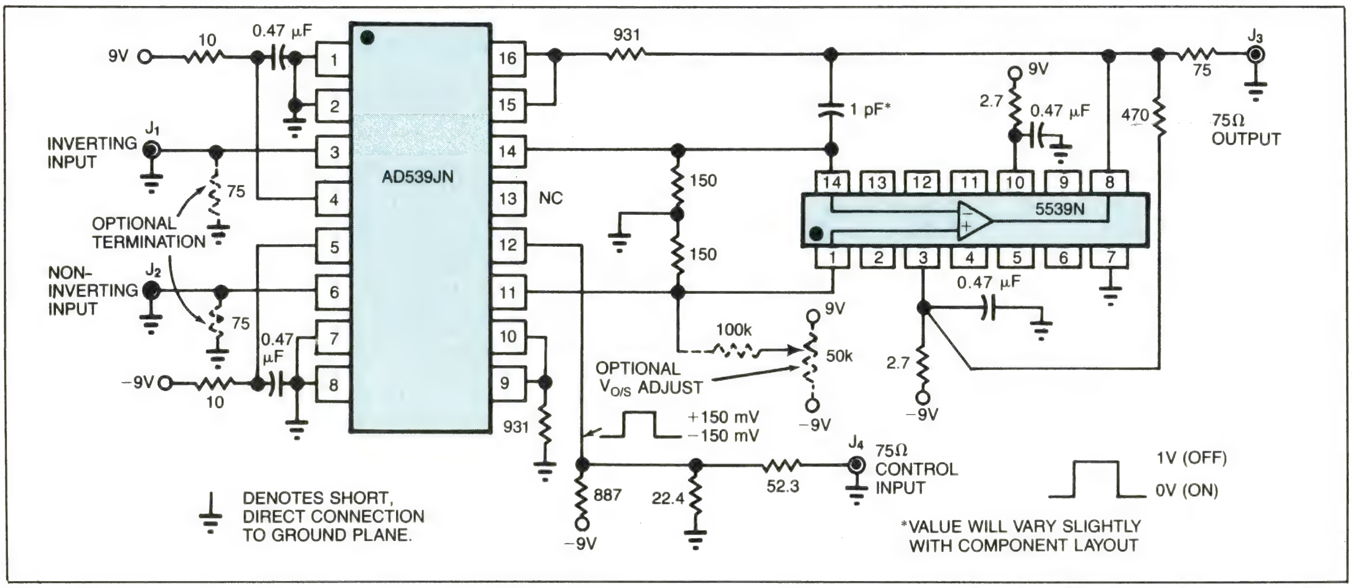


*Fig 1—**This high-speed spst analog switch** offers 50-nsec switching and a 30-MHz bandwidth.*

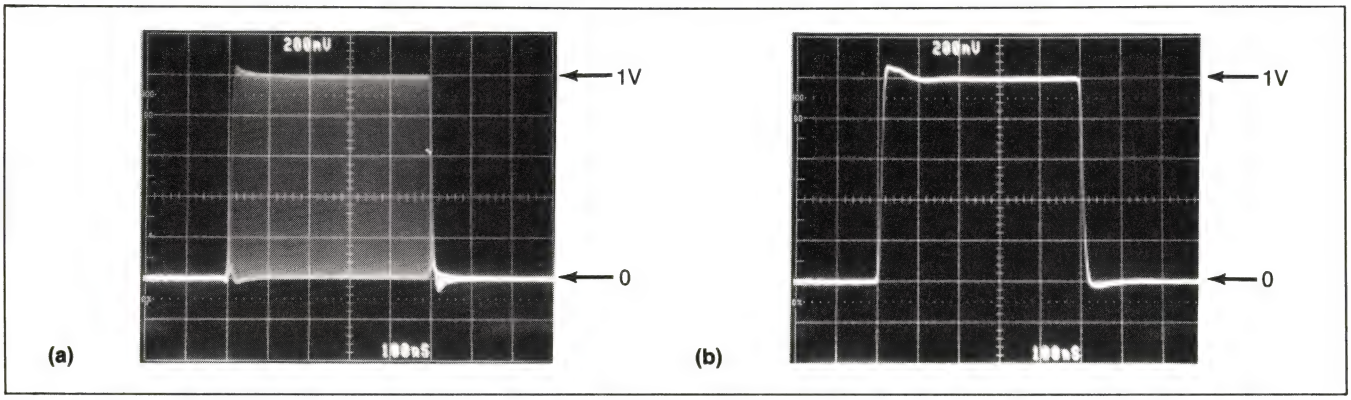


*Fig 2—**The output of the video switch in Fig 1** responds to a 0 to 1V sine wave applied to the noninverting input **(a)**; in **b**, the output responds to a 0 to 1V pulse at the noninverting input. Load resistance is 75Ω in both cases.*

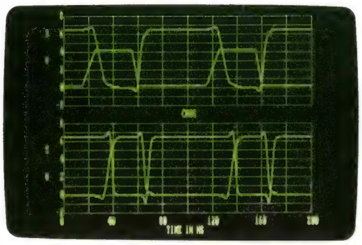
μC's EPROM allows on-line programming

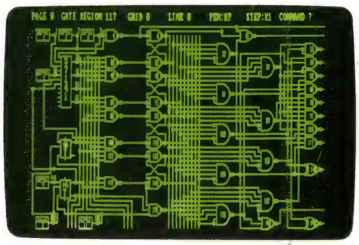
David R Gonzales
Motorola Inc, Austin, TX

The MC1468705G2 is a general-purpose CMOS microcomputer that requires a user-defined program in its EPROM. Before installing the μC, you program the EPROM using an on-line programming circuit **(Fig 1)**. (Program FF_{HEX} values in locations you wish to use for storage in the application program.)

Requirements for low current consumption in both

MICRO CAP and MICRO LOGIC put your engineers on line... not in line.


"Typical MICROCAP Transient Analysis"


"Typical MICROLOGIC Diagram"

How many long unproductive hours have you spent "in line" for your simulation? Well, no more. MICROCAP and MICROLOGIC can put you on line by turning your PC into a productive and cost-effective engineering workstation.

Both of these sophisticated engineering tools provide you with quick and efficient solutions to your simulation problems. And here's how.

MICROCAP: Your Analog Solution

MICROCAP is an interactive analog circuit drawing and simulation system. It allows you to sketch a circuit diagram right on the CRT screen, then run an AC, DC, or Transient analysis. While providing you with libraries for defined models of bipolar and MOS devices, Opamps, transformers, diodes, and much more, MICROCAP also includes features not even found in SPICE.

MICROCAP II lets you be even more productive. As an advanced version, it employs sparse matrix techniques for faster simulation speed and larger networks. In addition, you get even more advanced device models, worst case capabilities, temperature stepping, Fourier analysis, and macro capability.

MICROLOGIC: Your Digital Solution

MICROLOGIC provides you with a similar interactive drawing and analysis environment for digital work. Using standard PC hardware, you can create logic diagrams of up to 9 pages with each containing up to 200 gates. The system automatically creates the netlist required for a timing simulation and will handle networks of up to 1800 gates. It provides you with libraries for 36 user-defined basic gate types, 36 data channels of 256 bits each, 10 user-defined clock waveforms, and up to 50 macros in each network. MICROLOGIC produces high-resolution timing diagrams showing selected waveforms and associated delays, glitches, and spikes—just like the real thing.

Reviewers Love These Solutions

Regarding MICROCAP . . . "A highly recommended analog design program" (PC Tech Journal 3/84). "A valuable tool for circuit designers" (Personal Software Magazine 11/83).

Regarding MICROLOGIC . . . "An efficient design system that does what it is supposed to do at a reasonable price" (Byte 4/84).

MICROCAP and MICROLOGIC are available for the Apple II (64k), IBM PC (128k), and HP-150 computers and priced at $475 and $450 respectively. Demo versions are available for $75.

MICROCAP II is available for the Macintosh, IBM PC (256k), and HP-150 systems and is priced at $895. Demo versions are available for $100.

Demo prices are credited to the purchase price of the actual system.

Now, to get on line, call or write today!

Spectrum Software
1021 S. Wolfe Road, Dept. E
Sunnyvale, CA 94087
(408) 738-4387

CIRCLE NO 159

the normal and EPROM-programming modes are supported by the low-power op amp (used as a comparator) and by the transistors. These components also enable the µC to control the voltage applied to its V_{PP} input by means of the signal asserted at pin 11: The EPROM requires −13V at the V_{PP} input during programming and near 0V at V_{PP} when its code is being executed. Zener diode D_1 (13.5V) protects the EPROM by clamping negative-voltage transients. The 1-MΩ resistor on the V_{PP} control line ensures that, when the line is in a high-impedance state, it is near 0V during reset or power up.

Software for the programming operation **(Listing 1)** must reside in µC memory but not in the EPROM's address area. The µC allows program execution from any address in its memory map, so you must load a 2-instruction routine into the on-chip RAM; the routine (store the value to be programmed at the EPROM address; return to the main program) executes from RAM. An onboard timer allocates 20 msec per EPROM byte for programming and verification. **EDN**

To Vote For This Design, Circle No 747

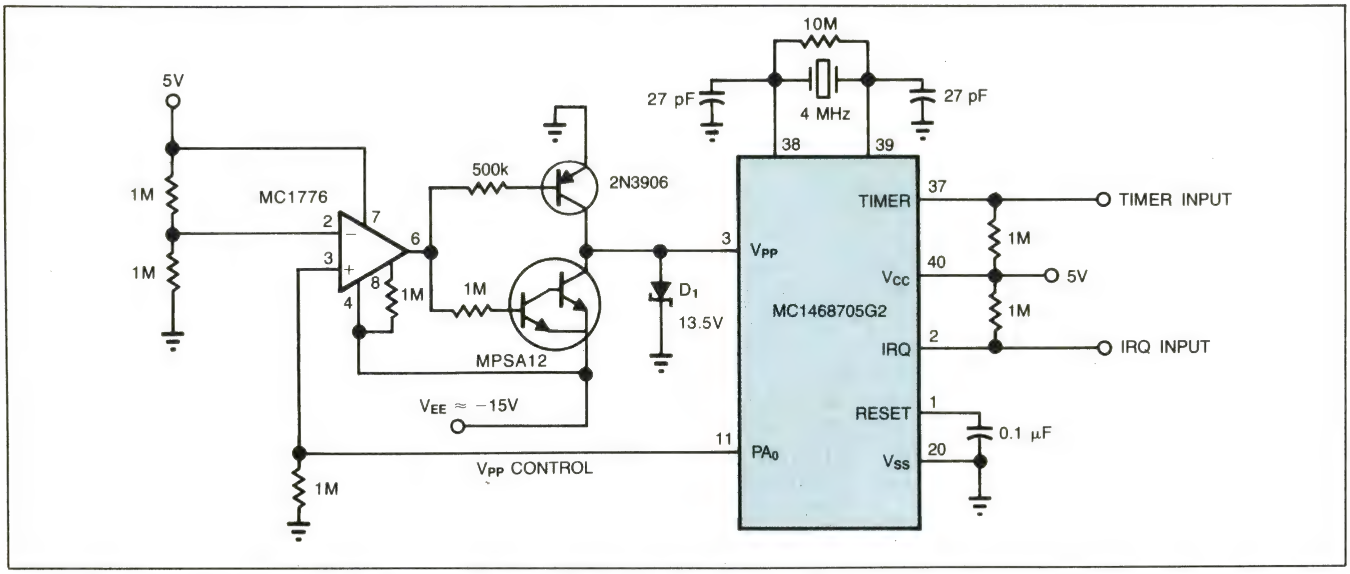


Fig 1—This circuit allows you to program the MC1468705G2 µC's onboard EPROM.

LISTING 1

```
                         opt   l            print assembly listing
0100           RomArea   equ   $100         Rom area start address
0010           RamSub    equ   $10          Ram area start address
0011           Address   equ   RamSub+1     address to program
0008           TmrData   equ   $08          Timer data address
0009           TmrCtrl   equ   $09          Timer control address
0000           PortA     equ   $00          porta data address

0100                     org   RomArea

0100 AE D7     ProgSub   ldx   #$D7         put (sta adrs,x) in ram
0102 BF 10               stx   RamSub
0104 AE 81               ldx   #$81         put (rts) in ram
0106 BF 13               stx   RamSub+3
0108 AE 47               ldx   #$47         clear tmr irq bit
010A BF 09               stx   TmrCtrl      select max prescaler
010C BE 50               ldx   80           10MS using 4MHZ clock
010E BF 08               stx   TmrData      for programming delay
0110 5F                  clrx               clear x register
0111 10 00               bset  0,PortA      enable VPP to MCU
0113 BD 10               jsr   RamSub       go program EPROM byte
0115 11 00               bclr  0,PortA      disable VPP to MCU
0117 81                  rts                return to main program
                         end
```

TEST INTERFACE

Sentry Link, a conversion program, transfers functional-test patterns that you have developed on the company's Logic Master design-verification system to the Fairchild Sentry tester. You can use these test patterns for device-characterization or volume-production tests. Logic Master interfaces to any CAE system's logic simulator. You can use this transfer package to determine if you have designed a device correctly and to ensure that it meets the requirements for high-volume production. The conversion program communicates with Sentry test system Models 7, 8, 10, 20, and 21. The software uses standard Sentry commands, including LSet, Enable, Set Module, Set F, and Set FC. An EPROM, which plugs into Logic Master, contains the program. $2950.

Integrated Measurement Systems, 9525 SW Gemini Dr, Beaverton, OR 97005. Phone (503) 626-7117.

Circle No 350

PERIPHERAL SUPPORT

AutoCAD now supports a variety of personal-computer peripherals. The graphics adapters that interface to this program are: the Bell & Howell Color Digital Imager IV, the Number Nine Revolution 512×8 controller, the Quintar Model 1080 & Graphport, the Frontier Bizgraph-1, the ACS Graphax 20/20, the Conographics Cono-Color 40, the BNW precision adapter, the Sigma Designs Color 400, and the Profit Systems Multigraph. Two mouse packages interface to the drafting package: the Torrington Manager Mouse and the Logitech Logimouse R-7. Four digitizing tablets—the Kurta Series II, the GTCO Micro Digi-Pad, the Mutoh CX3 Series, and the Calcomp 2100—also interface to the package. In addition, you can use the Ioline LP 3700 and the IBM 7300 Series plotters, as well as the Pencept Penpad 320 character-recognition system with the program. Basic package, $1000.

Autodesk Inc, 2320 Marinship Way, Sausalito, CA 94965. Phone (415) 332-2344.

Circle No 351

TEST FIXTURE

The combination of a Transgrid checkerboard universal grid and an interposing translator pc board can test pc boards having both on- and off-grid test points. Transgrid is a modification of a standard universal grid; half of the universal grid's pins and switching electronics have been removed to form a checkerboard pattern that leaves a pin in every other 0.001-in. location. The checkerboard grid contacts the underside of the translator board. The translator board, in turn, bears its own pins that contact the underside of the pc board under test. With the second translator board in place over the checkerboard grid, test points may be misaligned by as much as 0.150 in. from Transgrid's grid pins. An 8×10-in. bare-board test fixture with 600 points typically costs $550.

Testsystems Inc, 1045 W Geneva Dr, Tempe, AZ 85282. Phone (602) 894-9735. TLX 887866.

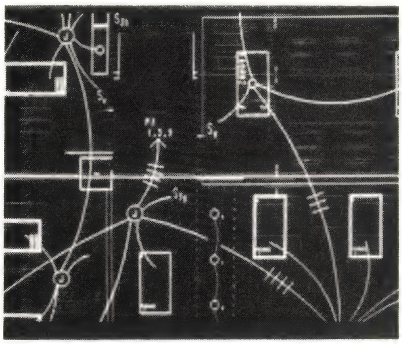
Circle No 352

PC-BASED CAE

The CDX-3100 and CDX-3150 CAE packages offer schematic capture as well as net-list extraction. The software packages run on IBM PC/ATs. The CDX-3150 package also includes the company's logic-simulator interface, which gives the system access to hardware accelerators, physical-modeling systems, and design compilation on a remote workstation. Because these packages interface to Ethernet, they both allow access to library resources on other network nodes. CDX-3100, $7900; CDX-3150, $9400 (10).

Cadnetix Corp, 5757 Central Ave, Boulder, CO 80301. Phone (303) 444-8075.

Circle No 353



ELECTRICAL DESIGN

EDP (electrical design package) aids in creating electrical plans for buildings, including lighting, power, and communication-system drawings. For use on this company's System 25 computer, the software features panel loading and balancing, automatic circuit ticking (ie, counting and displaying the number of wires in the conduit), automatic back-annotation of circuit numbers onto the desired items, and report generation. It also furnishes calculations of lighting requirements and fixture comparisons. The package performs six primary tasks. Electrical Setup creates a data file about a specific project or drawing. Components allows you to create electrical components and place them in a trial layout for analysis. Lighting determines the number of fixtures needed in a particular room and then places those fixtures. Circuiting allows you to connect all components into their appropriate circuits. Circuit Trace scans each circuit for configuration and loading updates, which are then stored. Fi-

THE BUS ARCHITECTURE CAREER COMPATIBILITY TEST.

Circle No 354

ASE PROGRAM

nal database program, , interfaces to the compa- cad software, runs on the nder MS-DOS, and facili- raction between the draw- ts associated data. The can transfer results to -3 and similar programs. ram's Infodata function ss-referenced information vidual objects and sym- Versacad drawing. The g processed blinks on the reen for positive identifi- can then change its prop- color, line style, and loca-

and save them to disk, and create a file that cross-references data attributes of various drawing objects. Functions include sorting operators such as And, Or, and Greater Than. $3000.

T&W Systems Inc, 7372 Prince Dr, Huntington Beach, CA 92647. Phone (714) 847-9960.

Circle No 355

DMA INTERFACE

The 4100F3Q DMA interface plugs into µCs that contain a Q Bus and a VS5XX-XB DMA interface. The interface consists of a single plug-in card, which contains the logic necessary to interface an external 16-bit-wide parallel device directly to the

Beaverton, OR 97075. Phone (503) 644-0161.

Circle No 356

OFFICE AUTOMATION

Designed to run on the company's 9000 Series 300 and 500 workstations, this technical office-automation software offers individual software programs or combination packages. The individual programs are Microtrak, Plottrak, TK Solver, Multiplan, Memomaker, Picture Perfect, and Diagraph. The integrated version, Alis, includes multifont word processing, sketching, graphics, a spreadsheet, business graphics, a personal database, an electronic-mail capability, network-

based information sharing, calendar management, meeting scheduling, and personal-time management. Alis, \$2500 to \$9000; individual packages for 9000 Series 300, \$195 to \$1550; individual packages for 9000 Series 500, \$1495 to \$2500. Delivery, three months ARO.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 357

GRAPHICS BOARD

The Ultragraph 800 graphics card runs on an IBM PC or PC/AT and furnishes a resolution of 800×400 pixels in 16 colors. The card automatically adjusts itself to emulate an IBM color-graphics board and thus allows you to run all IBM PC-compatible software. A character PROM generates text when running any PC-compatible software. The card has no jumpers or switches. It's designed to operate with the Microvitec 895 DU color monitor. Ultragraph 800, \$995; Microvitec DU, \$895.

Ultragraphics Corp, 37 S Franklin St, Chagrin Falls, OH 44022. Phone (216) 247-6600.

Circle No 358

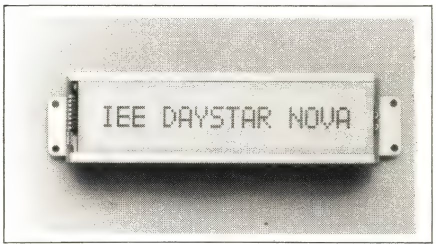
ACCELERATOR

The Turbosim logic-simulation accelerator is Zycad's Sprintor personal simulation package. The vendor has integrated this product into its IBM PC/AT-based CAE workstations. The accelerator can simulate >200,000 logical events/sec. \$8000.

Tektronix Inc, 5302 Betsy Ross Dr, Santa Clara, CA 95054. Phone (800) 547-1512; in OR, (800) 542-1877.

Circle No 359

CIRCLE NO 162



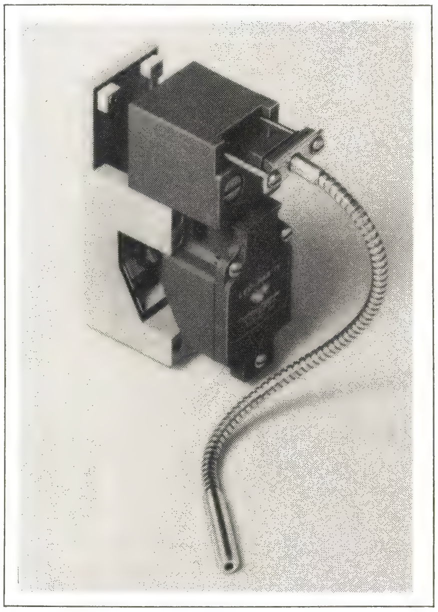
LCD

This Daystar Nova LCD has a 1-line×16-character display and offers both +20 and −20° preferential viewing angles for either top or bottom viewing. The display operates from −30 to +85°C. Optional electroluminescent backlighting permits use in complete darkness. The module includes a microcontroller with scrollable character RAM, and it can display as many as eight user-programmable characters. The characters are 0.36 in. high, so you can read them from as far away as 15 ft. The display package measures 5.4×1.5×1 in.; mounting brackets are included. The LCD accepts parallel ASCII data and commands via a user-selectable 8- or 4-bit data bus. The display's 5×7-dot matrix can display any of the 96 ASCII upper- and lower-case letters, numbers, and punctuation symbols, as well as scientific symbols. Operating requirements are 12 mA at 5V dc; the optional backlighting requires 125 mA at 5V dc. $73 (100).

IEE Inc, Industrial Products Div, 7740 Lemona Ave, Van Nuys, CA 91405. Phone (818) 787-0311. TWX 910-495-1707.

Circle No 360

INFRARED SWITCH



The LED-Pak IV miniature photoelectric switch combines microelectronics with fiber-optic noncontact sensing. Because the component is modular, you can assemble various configurations that permit simple mounting away from shock and vibration. Input power can be 115V ac, 230V ac, or 10 to 30V dc. Open-collector- and triac-output options are available. And, you have a choice of time-delay or one-shot operation. Sensors operate in opposed, reflective, and retroreflective modes. Various fiber-optic

DO YOU CHERISH MULTIPROCESSING LIMITATIONS?

Career Compatibility Test			
Bus Capability	*VME**	*MB II*	*Mark Your Preference*
Virtual Interrupts		*X*	
Number of Interrupt Levels	*7*	*255*	
Distributed Arbitration		*X*	
Number of Arbitration Levels	*4*	*20*	

Does the anguish of running out of interrupts give you a masochistic sense of pleasure?

If so, stay away from the MULTIBUS® II architecture.

Because of its virtual interrupt feature, MULTIBUS II boards give you all the sources and destinations of interrupt you need for multiprocessing. Up to 255.

And to make it an even stronger candidate for multiprocessing, the MULTIBUS II architecture features distributed arbitration. Which assures that no single board can hog the bus. In fact, MULTIBUS II systems are so flexible they can easily accommodate up to 20 bus masters.

Of course, if you believe that needless frustration builds character, you should choose the other bus.

You'll be stuck with a dedicated interrupt arrangement that effectively allows you only seven interrupts. And because it uses central arbitration, you're effectively limited to only four masters.

Of course, if you want to design systems that are more powerful, useful and flexible, you should choose the MULTIBUS II architecture.

Now turn to the last page and complete the test.

*Source: IEEE P1014 Draft 1.2, August 1985.

CIRCLE NO 201

scanners are available for remote control. From $100.

Dolan-Jenner Industries Inc, Box 1020, Woburn, MA 01801. Phone (617) 935-7444. TLX 948161.

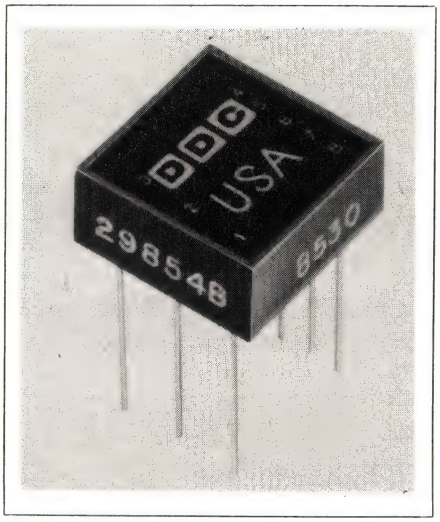
Circle No 361

F-O MODULES

These high-performance fiber-optic transmitters and receivers come in corrosion-resistant packages and include photodiodes characterized by low capacitance, low dark current, and high responsivity, according to the manufacturer. The laser-based transmitter devices are compatible with 1.3-μm fiber-optic systems using single-mode fibers. They operate at data rates to 565M bps and spec an optical output to −1 dBm. The transmitters use an injection laser, a photodiode monitor, interface circuitry, and a thermoelectric cooler. Each laser diode comes with a single-mode fiber pigtail and a single-mode, fiber-optic biconic-connector termination. Four receiver devices are available. They are designed for use in 1.3- to 1.55-μm long-wavelength communication systems and operate at data rates as high as 417M bps with sensitivities to −52 dBm. Transmitters, $4500 to $5760; receivers, $1600 to $3000. Delivery, 14 to 16 weeks ARO for production quantities.

AT&T Technology Systems, 1 Oak Way, Rm 2WC-106, Berkeley Heights, NJ 07922. Phone (800) 372-2447.

Circle No 362



TRANSFORMER

You can use the BUS-29854 transformer with a MIL-STD-1553 serial mux data bus. This pulse transformer provides all of the turns ratio, component isolation, and common-mode rejection characteristics required of Manchester II serial 2-phase data transmission. It has a turns ratio of 1:0.83 and 1:0.60; operating range is −55 to +125°C. The transformer rises 0.275 in. above the circuit board. It's packaged in accordance with MIL-T-21038 and is compatible with the manufacturer's BUS-63107 Series

data-bus transceivers. The tin-coated steel leads accommodate pc-board mounting. The device processes sinusoidal or trapezoidal waveforms in accordance with MIL-STD-1553. $35. Delivery, eight weeks ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 510-228-7324.

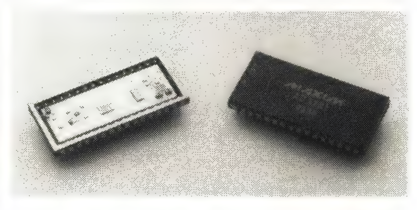
Circle No 363

AMPLIFIER/DETECTOR

Model ICE1000 is a 1-GHz linear amplifier/detector with a 500-MHz bandwidth and a 15-nsec rise time. Designed primarily for radar and other applications requiring high-speed IF processing, the device incorporates an ac-coupled video detector, which has 60 dB of gain and a 20-dB dynamic range. The video output can drive 93Ω loads to 2.2V nominal. The device is packaged in a 4.625×1.5×0.47-in. housing. It meets MIL-E-5400/MIL-E-16400 environmental requirements. $1750. Delivery, 120 days ARO.

RHG Electronics Laboratory Inc, 161 E Industry Court, Deer Park, NY 11729. Phone (516) 242-1100. TWX 510-227-6083.

Circle No 364



A/D CONVERTERS

The AD578S 12-bit A/D converter works over the full military temperature range and specs a conversion time of 4.5 μsec. The AD578J, -K, and -L family members operate over 0 to 70°C with conversion times of 6, 4.5, and 3 μsec, respectively. The converters exhibit 12-bit accuracy with no missing codes over temperature. Nonlinearity is <¾ LSB max (AD578J, -K, -L) over 0 to 70°C and <1 LSB max (AD578S) over −55 to +125°C. At 25°C, gain error is 0.25% of full scale, with a temperature coefficient of 30 ppm/°C. The offset is 0.25% of full scale at 25°C, and the temperature coefficient is 10 ppm/°C for unipolar offset and 20 ppm/°C for bipolar offset. The devices are housed in 32-pin ceramic DIPs. $119.75 (100).

Maxim Integrated Products, 510 N Pastoria Ave, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 365

HEAT SINKS

Series 5197-5201 heat sinks replace cast-aluminum heat sinks, reducing costs by 30 to 40% and also reducing package size. Each device is stamped from ⅛-in.-thick aluminum and is designed for use with TO-3,

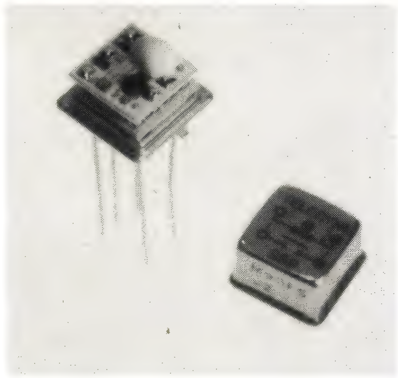
TO-66, TO-220, TO-218, and similar devices. Measuring 1.900 in. long and 1.550 in. wide, the devices are available in four heights from 1.225 to 2.00 in. The finned design provides free circulation of air from all sides. With an input of 10W, the smallest heat sink has a 50°C rise above ambient under natural convection. You can mount the semiconductor and a heat sink to the pc board with the same screws. The heat sinks are available in several finishes, including black, bronze, blue, or red anodized, as well as gold chromate. $0.637 (1000).

Aavid Engineering Inc, Box 400, Laconia, NH 03247. Phone (603) 524-4443.

Circle No 366

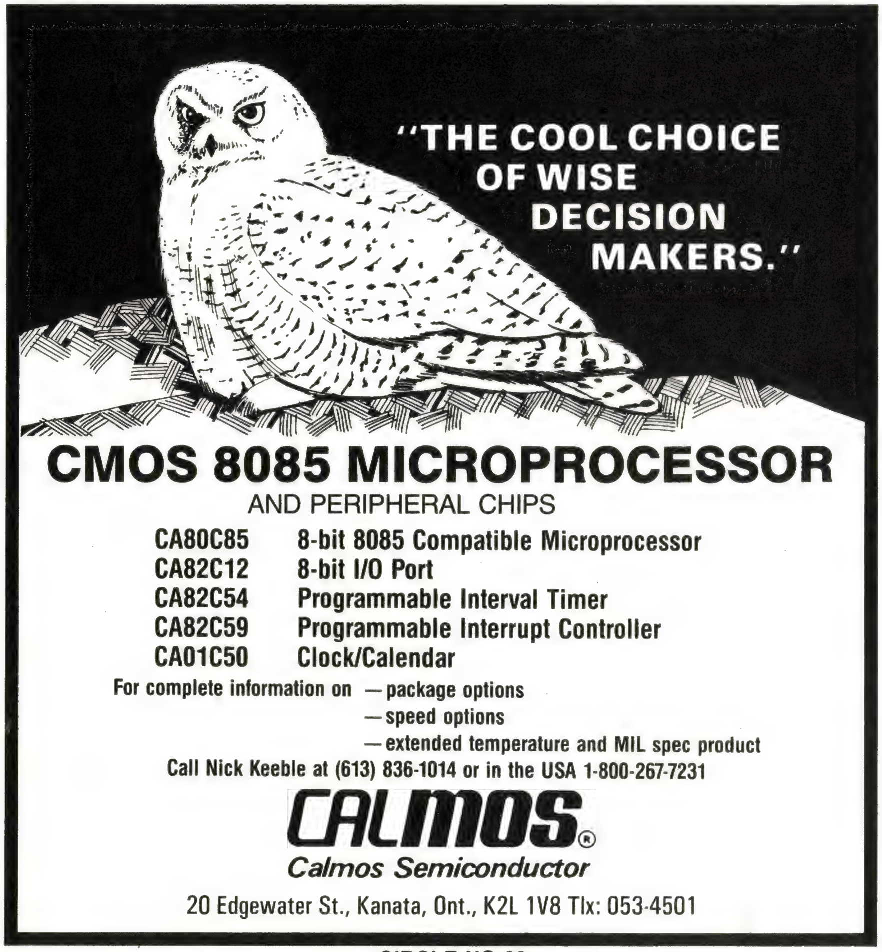
POWER FET HYBRIDS

The M90FS-2 and M85FS-2A power FET switching hybrids are designed to replace electromechanical relays in such applications as low-level and high-voltage switching applications, where short-circuit conditions are expected. Short-circuit protection operates during switching into a dead short, and when a short circuit is applied during normal operation. In either case, the unit will sense the short-circuit condition and initiate current limiting



and total shutdown, typically within 200 msec. The unit will then block the short-circuit condition indefinitely until the short is removed and the unit is reset, either by cycling the input control or taking the load voltage to zero. A custom IC will also sense current-overload conditions and prevent damage from thermal runaway due to excessive load current or ambient operating temperatures. The M90FS-2 is rated at 1A (25°C) at 60V and is

CIRCLE NO 27

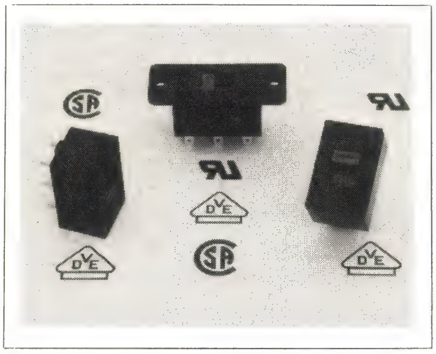


CIRCLE NO 28

housed in a hermetically sealed low-profile package. The M85FS-2A is electrically equivalent to the M90FS-2, but is housed in a hermetically sealed 14-pin metal DIP, which doubles the current-carrying capacity and allows 2.1A operation at 25°C and 1.2A operation at 80°C ambient temperature. \$94 to \$125 (250). Delivery, four to six weeks ARO.

Teledyne Solid State, 12525 Daphne Ave, Hawthorne, CA 90250. Phone (213) 777-0077.

Circle No 367



SLIDE SWITCHES

V Series slide switches have VDE, UL, and CSA approval. Available in spst, spdt, dpst, and dpdt versions with silver-plated contacts and terminals, the switches come in four terminal styles, including printed circuit and quick connect. Two actuator styles come in red or black; some models include voltage markings on the actuator. Actuator material is glass-filled polyester (UL 94V-0). Housing with or without mounting ears is black 6/6 nylon (UL 94V-2). UL/CSA rating specs at 10.1A at 125V ac and 5A at 250V ac. VDE rating is 2A at 250V ac resistive and 0.5A at 250V ac motor load. Initial contact resistance is less than 10 mΩ typ, and insulation resistance is $10^9\Omega$ min. Single-pole models, \$0.85; double-pole models, \$1.25 (1000).

C&K Components Inc, 15 Riverdale Ave, Newton, MA 02158. Phone (617) 964-6400.

Circle No 368

The newest concept in data acquisition: one of these and one of these and a little bit of this.

The Digitec MagnumPC™ combines datalogging, menu set-up, graphics, reports, analysis, control.

It's so easy to set up and so easy to use, you already know everything you need to get working.

The MagnumPC's dICON software is user definable and menu driven to lead you easily through set-up from one step to the next. Right out of the box. Without programming.

You can customize alphanumeric reports, line graphs and bar charts, both real-time and historical. And the display menus define both the hardware installation and application for measurement, control, analysis and reporting.

The MagnumPC gives you a throughput of 30 to 50 channels per second; it's ideal for 50 to 100 channel applications, with up to 1000 channels available.

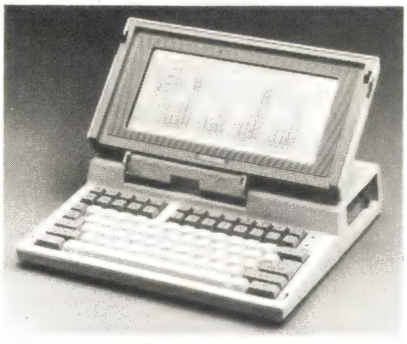
And no other system that gives you so much costs you so little. A MagnumPC system can be configured for as little as $4,400. Compare feature for feature, compare ease of set-up and use, and you won't find a better price anywhere.

Now you know all it takes to run the Digitec MagnumPC system. Here's everything you need to know to get yours. Write: 918 Woodley Road, P.O. Box 458, Dayton, Ohio 45401-0458. Phone (513) 254-6251; telex 687-5219-WUI.

Quality, service, flexibility, economy.

DigiTec

CIRCLE NO 165



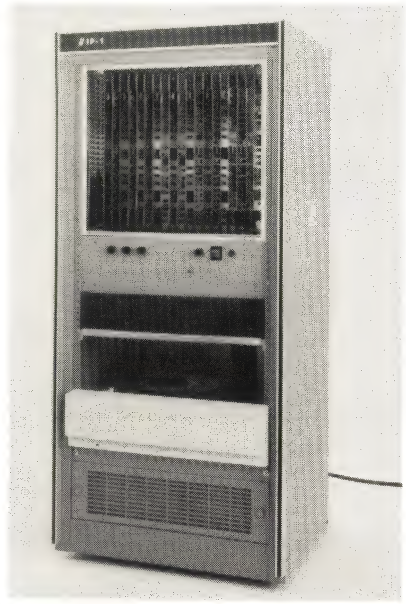
LAP COMPUTER

The T1100 lap computer gives you IBM PC compatibility in a 9-lb portable unit. Standard features include 512k bytes of RAM; a 720k-byte, 3½-in. floppy-disk drive; and the MS-DOS operating system. You can adjust the viewing angle of its 80-character×25-line LCD, which has a 640×200-pixel resolution. A built-in rechargeable NiCd battery delivers four to eight hours of power. The unit includes an 83-character keyboard, a color-monitor interface, a parallel-printer port, and an interface for a second floppy-disk drive. An ac adapter, user manuals, and carrying case complete the package. Options include 3½-in. and 5¼-in. external floppy-disk drives; a printer; and a multifunction card with a 300-bps modem, calendar/clock, and an asynchronous communications port. $1999.

Toshiba America Inc, Information Systems Div, 2441 Michelle Dr, Tustin, CA 92680. Phone (714) 730-5000.

Circle No 369

PARALLEL PROCESSOR



Featuring nine CPUs in its basic configuration, the IP-1 parallel-processing computer runs at speeds from four to 20 MIPS with full 32-bit addressing. It uses a real-time, multiuser operating system, Runix, which implements the Unix kernel functions. Also provided in the standard software package is an intercomputer communications program. Other standard features include a 10M-byte main memory, expandable to 40M bytes; 150M bytes of disk storage; more than 50 I/O

Sheer performance in emissions control.

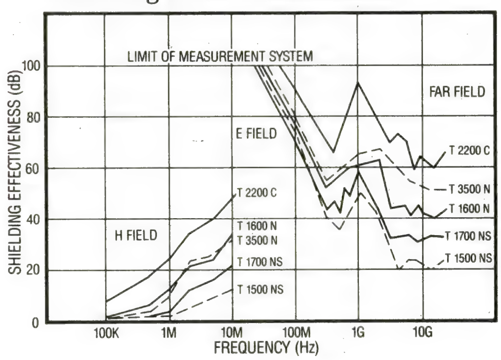
If you're looking for flexible new solutions for your TEMPEST, EMI and ESD control problems, take a look at TexGuard.

Lightweight, breathable and extremely versatile, TexGuard metalized fabrics come in a wide variety of transparent and opaque styles that can be easily tailored to fit your design needs. Available in sheets and rolls, the fabric can also have waterproof or adhesive backing. TexGuard fabrics are polyester based, then plated with a thin deposit of copper, nickel or other metal. By combining the type of fabric, type of metal and depth of plating, precise electrical properties can be economically obtained for your specific application.

TexGuard fabrics can provide 50 dB or more of attenuation in the 0.1 to 1000 MHz frequency range and up to 48 dB in the 1 to 21 GHz range.

So whether your application involves shielding individual components — or entire environments — look into TexGuard.

Shielding Effectiveness Chart



For a complete technical package including product samples and shielding effectiveness specifications call the High Performance Textile Division of TW Trading International at 408/429-1304 or write:

TexGuard™

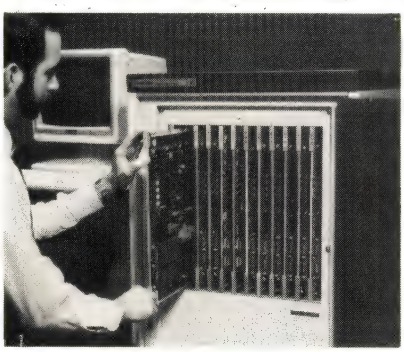
303 Potrero Street, Suite 17
Santa Cruz, CA 95060 TELEX 296696 TWT UR

CIRCLE NO 166

ports; a CRT terminal; and interfaces for printers, plotters, disk drives, and tape drives. Options include the FPA-32, a floating-point processor with a peak-performance rating of 160M flops, and CAD routing software. IP-1, $49,950; FPA-32, $74,000. Delivery, two to four months ARO.

International Parallel Machines Inc, 700 Pleasant St, New Bedford, MA 02740. Phone (617) 990-2977.

Circle No 370



PARALLEL COMPUTER

Well-suited for parallel-processing applications in environments with limited space, the Series 600 Flex/32 multicomputer gives you a multiple bus structure in a set of 21-in.-high, 19-in.-wide rack-mountable card cages. You can add 32-bit processing power, memory, and I/O bandwidth as your processing needs increase. Furthermore, software developed on your Series 600 system can run without alterations on any other Flex/32 Series computer. These computers operate within a multiple instruction stream, multiple data stream, and multiple I/O stream environment for execution flexibility. Software available for this system includes Unix System V, Ada, MMOS (multicomputing multitasking operating system), and a Concurrency simulator to test parallel applications. From $50,000.

Flexible Computer Corp, 1801 Royal Lane, Bldg 8, Dallas, TX 75229. Phone (214) 869-1234. TWX 510-600-1569.

Circle No 371

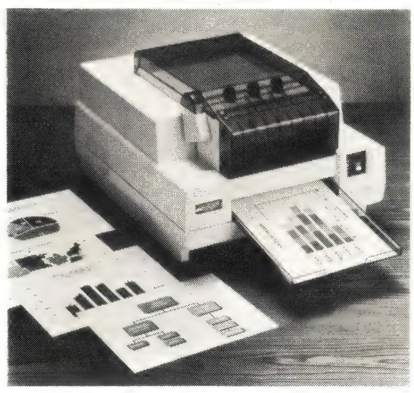
PLD PROGRAMMER

The iPLDS, a computer-hosted development system for erasable programmable-logic devices, comes with software, programming hardware, an interface for an IBM PC, and sample programmable devices. This system lets you develop, program, and test a logic design in a matter of hours. The system's software tools incorporate techniques used in CAE workstations and software development processes. The tools let you perform design entry, logic optimization, compiling, automatic design fitting, and hardware verification. You can use several design-entry methods, including direct Boolean-equation entry, schematic-capture packages, state-

machine entry, and an interactive net-list entry package called Logic Builder. Interactive graphics, menus, user prompts, and help messages simplify system use. $2500.

Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. Phone (503) 681-2279.

Circle No 372



PLOTTER

The Colormaster thermal-transfer plotter/printer, with a built-in rasterizer, lets you produce 7-color graphics on plain paper or acetate. The rasterizer, with its 512k-byte buffer, frees the host computer from the task of converting graphics and text to raster data. The printer/plotter can generate seven colors by overlaying dots in three colors—yellow, magenta, and cyan. You can make a color copy of an A-size page in approximately 1.5 minutes or a monochrome copy in 45 sec. The unit can automatically print as many as 100 plain-paper copies and as many as 50 acetate copies. Horizontal resolution is 203.2 dots/in. and vertical resolution is 200 dots/in. The printer/plotter feeds the paper onto a drum, which rotates the paper in front of a thermal head and ribbon. The head elements melt the ink on the ribbon to form a permanent image on the paper. $4495.

Calcomp, 2411 W La Palma Ave, Anaheim, CA 92801. Phone (714) 821-2142.

Circle No 373

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It means the end of battery-related product complaints.

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To add even more value, consider that you won't face position-related design problems. dryfit batteries are made to operate and recharge in any position—even upside down! They are also deep discharge protected for up to 30 days and have a low self-discharge rate of approximately 0.1% per day at 20°C.

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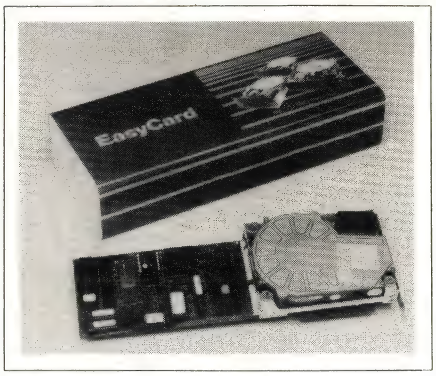
CIRCLE NO 169



HARD-DISK DRIVE

The Easycard uses one slot in your IBM PC or compatible computer to add 20M bytes of storage to your computer. The drive's unformatted capacity is 25.52M bytes. It boasts a data-transfer rate of 5M bytes/sec and an average access time of 80 msec. The closed-loop servo-positioning system microsteps the heads for read/write positioning accuracy; therefore, you don't have to worry about thermal expansion, hysteresis of the stepper motor, or mechanical wear. Using less than 9W of power during normal operation, the disk drive requires no auxiliary or upgraded power supply. It contains a μP, which tests the drive when you apply power and makes repeated checks of the drive's performance during operation. $1095.

Microscience International Corp, 575 E Middlefield Rd, Mountain View, CA 94043. Phone (415) 961-2212. TLX 275907.

Circle No 374

TAPE DRIVE

Featuring quad density, the FS2000 ½-in. streaming-tape drive provides as much as 270M bytes of data-storage capacity. An automatic loading feature frees you from tape handling. The drive also performs its own read-gain, write-current, and de-skew adjustments. It has 13 VLSI chips, which help to minimize size: The drive is 8.75×22×19 in. Internal diagnostics, user-selectable operating speeds, and the drive's linear power supply increase data reliability and system flexibility. You can order a 256k-byte cache memory to maximize the drive's data burst rate to 1M bytes/sec. From $5850 (250).

Pertec Peripherals Corp, Box 2198, Chatsworth, CA 91311. Phone (213) 882-0030. TWX 910-494-2093.

Circle No 375

WINCHESTER DRIVE

Providing 800M bytes of unformatted storage capacity, the D2362 has seven 9-in. platters and an average access time of 15 msec. The Winchester disk drive incorporates thin-film plated media and has a rotation speed of 3600 rpm and a data-transfer rate of 2.46M bytes/sec. Spindle support at both ends increases the drive's read/write accuracy. The drive's MTBF rating is 20,000 power-on hours; mean time to repair is less than one hour. Approximately $8000 (100).

NEC Information Systems Inc, 1414 Massachusetts Ave, Boxborough, MA 01719. Phone (617) 264-8000.

Circle No 376

OPTICAL STORAGE

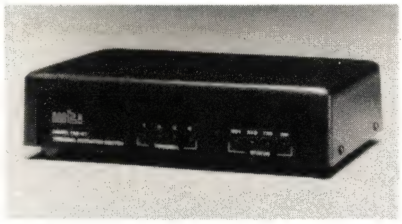
The BP-100+ portable data-storage unit lets you store as much as 100M bytes of information on a single write-once, removable optical disk. The disks provide a permanent record of your data files and allow you to read any one disk repeatedly without data degradation. The unit has a data-transfer rate of 2.5M bps and an average access time of 200 msec. It weighs 6 lbs and fits in a briefcase. You can connect it to any IBM PC or compatible computer via an Adaptacon I/O extender board. The unit comes with a collection of menu-driven software utilities for backup and restore operations. $5000.

Portable Solutions Inc, 1701 Directors Blvd, Suite 250, Austin, TX 78744. Phone (512) 448-4965.

Circle No 377

4-PORT SWITCH

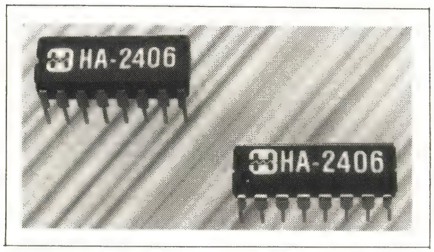
The TAS-41 terminal-activated switch allows four users to share one computer port. Each user can access the computer by entering



commands from a remote terminal's keyboard. If another person is already using the port, the user attempting access will receive no response from the system until the port sends a "port available" message. To prevent the port from remaining unavailable in the event that a user forgets to log off a terminal, a time-out feature automatically disconnects a port if no data activity occurs within a user-selectable time period. $395.

Western Telematic Inc, 2435 S Anne St, Santa Ana, CA 92704. Phone (800) 854-7226; in CA, (714) 979-0363.

Circle No 378



4-CHANNEL OP AMP

The HA-2406 operational amplifier features four digitally selectable, TTL-compatible inputs tied to one output stage. This device combines the functions of an analog switch and a quad op amp on a monolithic chip. You can configure the chip as a programmable-gain amplifier, programmable filter, analog multiplexer, or 4-channel multiplexer, as well as other programmable analog functions in digitally controlled processing systems. Each input channel has a 20V/μsec slew rate and a 30-MHz gain bandwidth. Crosstalk rejection is −110 dB, offset voltage is 7 mV, and bias current is 50 nA. The device operates over 0 to 75°C and is available in a plastic or ceramic 16-pin DIP. $2.40 (100).

Harris Corp, Semiconductor Products Div, Box 883, Melbourne, FL 32919. Phone (305) 724-9100.

Circle No 379

DYNAMIC RAMs

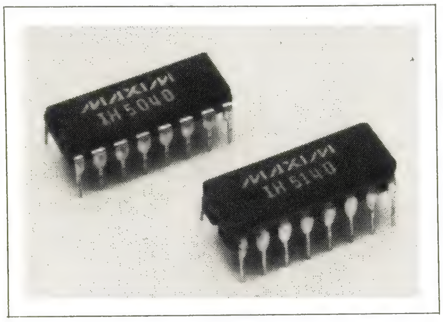
These static-column dynamic RAMs, the MB81C258 and the MB81C466, have a density of 256k bits and are organized as 256k×1 bit and 64k×4 bits, respectively. Processed in CMOS technology, both devices are available with row-access times of 100, 120, or 150 nsec; in static-column mode, respective address-access times are 35, 45, and 55 nsec. At 150 nsec, active maximum current is 45 mA and standby current is 0.2 mA. The MB81C258 is a page-mode part; the MB81C466 is a nibble-mode part. MB81C258, $10.25 (150-nsec version), $12.25 (120-nsec version), and $15.25 (100-nsec version) (100); MB81C466, $11.25 (150-nsec version), $13.25 (120-nsec version), or $16.25 (100-nsec version) (100). Samples are available now; production quantities are scheduled for 2nd qtr.

Fujitsu Microelectronics Inc, Integrated Circuits Div, 3320 Scott Blvd, Santa Clara, CA 95054. Phone (408) 727-1700. TWX 910-338-0190.

Circle No 380

ANALOG SWITCHES

The IH5040 and IH5140 families of CMOS analog switches both consist of latch-up-proof, break-before-make, single and dual versions of spst, spdt, and dpdt formats. Each family contains six devices, which are differentiated according to the type of switch action. The switches spec a low off-state leakage current of 1 nA max and a quiescent current of <1 μA. IH5040 parts switch at



400 nsec (t_{ON}) and 200 nsec (t_{OFF}). Model IH5140M's t_{ON} switching time is 100 nsec max; t_{OFF} is 75 nsec. Current-limiting circuitry prevents device damage even if the supplies are grounded and the input voltages are still connected. All switches are bidirectional and maintain almost constant on-resistance (75Ω typ) over the output-voltage operating range. The company guarantees that both families operate from ±4.5 to ±18V supplies. IH5040 family, $2.74 to $15.55; IH5140 family, $4.07 to $20.70 (100).

Maxim Integrated Products, 520 N Pastoria Ave, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 381

MICROCONTROLLER

The HD63701V0P, the second microcontroller chip in the ZTAT (zero turn-around time) family, has a 4k-byte 1-time-programmable EPROM, an asynchronous serial communications interface, 29 parallel I/O pins, and a 16-bit programmable timer. Operating at 1, 1.5, or 2 MHz, it is upward compatible with the company's 6801. This CMOS device is pin-for-pin compatible with the HD6301V1P masked-ROM, the HD63701V0C reprogrammable device, and the HD63P01M1 piggyback device. It contains 192 bytes of RAM, as compared with the masked-ROM and piggyback devices' 128 bytes. ZTAT microcontrollers allow manufacturers to avoid typical 3- to 4-month turnaround times, as well as the high mask charges, minimum-order restrictions, and work-in-progress liability associated with masked-ROM devices. Enclosed in a 40-pin plastic DIP, it costs $11.80 (1000).

Hitachi America Ltd, Semiconductor & IC Div, 2210 O'Toole Ave, San Jose, CA 95131. Phone (408) 942-1500. TWX 910-338-2103.

Circle No 382

TONE DETECTOR

The MV8870, a DTMF single-chip receiver, integrates band-split-filter and digital-decoder functions, as well as a differential-input amplifier, clock oscillator, and 3-state outputs on one chip. The filter section uses switched-capacitor techniques for high- and low-group filters and dial-tone rejection. Using digital-counting techniques for detect and decode, the device decodes all 16 DTMF tone pairs into 4-bit code. $6.65 (1000).

Plessey Semiconductors Inc, 3 Whatney, Irvine, CA 92718. Phone (714) 951-5212.

Circle No 383

STATIC RAM

The V62C64 is a low-power, CMOS static RAM organized as 8k×8 bits. Pin-compatible with industry-standard devices, the RAM specs a 150-nsec access time and dissipates 175 mW while operating and 4 μW in data-retention mode. The data-retention mode is useful in applications requiring battery backup. The RAM uses 4-transistor cells and comes in an SO package or 24-pin DIP. $4.66 (DIP); $4.86 (SO package) (100).

Vitelic Corp, 3910 N First St, San Jose, CA 95134. Phone (408) 433-6000. TLX 3179461.

Circle No 384

CMOS EPROM

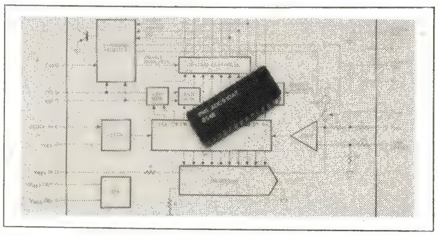
The MBM27C512 is the first 512k-bit EPROM to use CMOS technology. According to its manufacturer, it offers the lowest power per bit of any EPROM: Maximum standby power is 0.525 mW as compared

with 210 mW for a typical NMOS part. The device has industry-standard, JEDEC-compatible pinouts and a standard 12.5V programming voltage. You can choose from three speed options: 200, 250, or 300 nsec; you can also choose between two packages: a ceramic DIP or a ceramic leadless chip carrier. $50 (100).

Fujitsu Microelectronics Inc, 3320 Scott Blvd, Santa Clara, CA 95054. Phone (408) 727-1700. TWX 910-338-0190.

Circle No 385

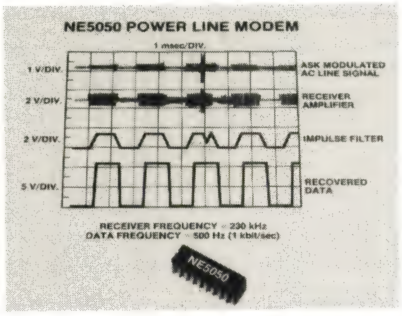
A/D CONVERTER



Offering output data in either a 10-bit parallel format or an 8-bit-byte format, the ADC-910 10-bit A/D converter completes conversions in 6 µsec max. The µP-compatible device contains a 10-bit D/A converter, a successive-approximation register, a 2.5V bandgap reference, a clock, 3-state output buffers, a programmable control register, and a status register. Integral-nonlinearity and zero errors are specified at ±½ LSB over temperature; the spec also guarantess no missing codes over temperature. Microprocessor interfacing takes place through a multiplexed bidirectional data port; you control the data with chip-select lines in combination with standard processor read/write lines. Available in a 28-pin DIP for operation over commercial, industrial, or military temperature ranges, the ADC-910 costs $18.45 (100).

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. TWX 910-338-0218.

Circle No 386



MODEM IC

The NE5050 modem IC is suited for power-line and twisted-pair communications and offers high immunity to transmission noise and impedance variations. Containing an independent transmitter and receiver, the device transmits and receives by on/off carrier modulation (amplitude-shift-key (ASK) modulation). The IC provides 100k-bps data rates (except in applications using power-line communications, which dictate lower data rates because of noise-immunity considerations). The device can perform carrier-sense, multiple-access/collision detection (CSMA/CD). The receiver portion of the IC has 1-mV sensitivity. The receiver's input amplifier provides protection against input transients as high as 30V p-p. Operating from a 12V supply, the modem IC draws 10 mA in standby mode. In a 20-pin plastic DIP, $1.95; in an SO, surface-mount package, $2.15 (100).

Signetics Corp, Box 3409, Sunnyvale, CA 94088. Phone (408) 991-4577.

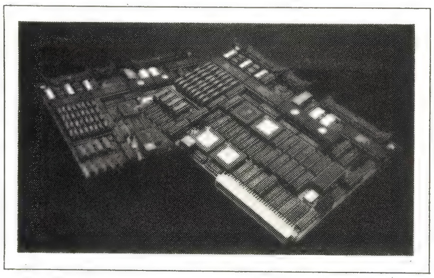
Circle No 387

D/A CONVERTER

Offering a voltage output, the HS33806 4-quadrant multiplying D/A converter operates over the military temperature range. The converter eliminates the need to add external op amps and resistors for conversion to voltage output. Housed in a 28-pin double DIP, the device has a double-buffered input whose first rank is configured as three independent, 4-bit bytes; this configuration permits direct interface with 4-, 8-, and 12-bit data buses. Full-scale transition settling time is 5 μsec max, integral nonlinearity is ±0.015% full-scale range max, and differential nonlinearity is ±0.024% full-scale range max. Monotonicity to 12 bits is guaranteed over the full temperature range. The small-signal and full-power bandwidths for the reference input are 500 and 200 kHz, respectively. Power consumption is 405 mW typ. Screening to MIL-STD-883, Revision C, Level B, is available. $110 (100).

Hybrid Systems Corp, 22 Linnell Circle/Suburban Industrial Park, Billerica, MA 01821. Phone (617) 667-8700.

Circle No 388



VME COMPUTER BOARDS

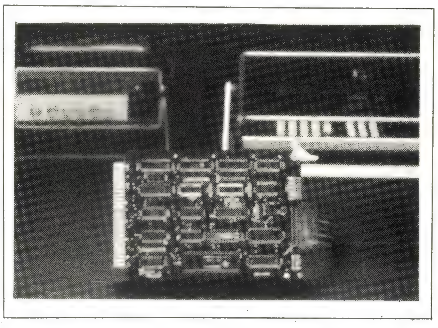
The HK68/V family of VME Bus μC boards comprises the HV68/V10 board for systems running Unix and the HK68/VE board for real-time systems. The HK68/V10 contains a 68010 μP that can access as much as 1M byte of onboard RAM and 128k bytes of EPROM. For I/O operations, the board includes a 4-channel DMA controller, two serial ports, a SCSI interface that's capable of connecting as many as eight peripherals, and mailbox-interrupt capability. For coprocessing, you can insert a 68881 floating-point processor, and you can order the board with a memory-management unit. The HV68/VE board includes the same processor and memory configuration as the HV68/V10, but the DMA controller is optional to make the board less expensive for real-time processing. The HV68/VE also comes with two serial ports, 20 parallel I/O lines, mailbox-interrupt capability, and a socket for the 68881. From $895 (100).

Heurikon Corp, 3201 Latham Dr, Madison, WI 53713. Phone (800) 356-9602; in WI, (608) 271-8700. TLX 469532.

Circle No 389

GPIB-STD BUS LINK

You use the CDI-488 board to link the IEEE-488 (GPIB) bus with the STD Bus. Based on the TMS 9915 GPIB-adapter IC, the board connects to both buses and is compatible with STD Bus CPUs and IEEE-488 standards. The board functions



on the buses as a talker, listener, or controller device. Other devices on the buses can either interrupt or poll the board for interbus transactions; you can implement vectored, daisy-chained, or externally prioritized interrupts. Transfer rate is 1M byte/sec max and between 250k and 500k bytes/sec typ. The board includes software-addressable, GPIB address switches and eight GPIB status indicators. $300.

Computer Dynamics Inc, 105 S Main St, Greer, SC 29651. Phone (803) 877-7471.

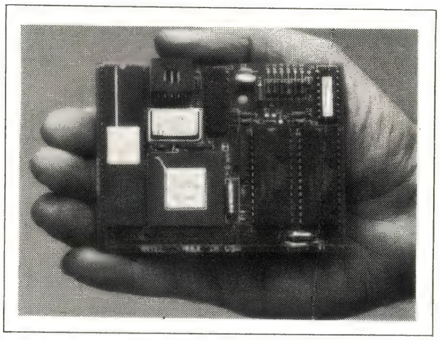
Circle No 390

ANALOG INPUT BOARD

Transformers provide 900V of isolation between the MP8450's 16 inputs and your Multibus system. The board also provides 700V channel-to-channel isolation. The 9-Hz low-pass filter on the inputs detects open circuits. You can program the amplification of each channel by installing resistors on the board. Input-voltage range can vary from ±10 mV to ±5V. The board's 20-bit address can reside in either memory or I/O space within the Multibus system. $1650.

Burr-Brown Corp, Data Acquisition and Control Systems Div, 3631 E 44th St, Tucson, AZ 85713. Phone (602) 747-0711. TWX 910-952-1111.

Circle No 391

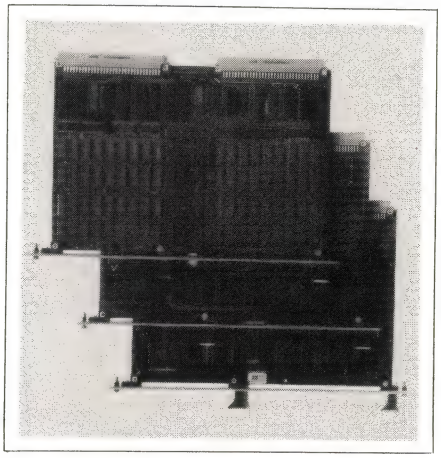


ETHERNET BOARD

The iSBX 586 Ethernet Data Link Engine attaches to any iSBX bus-compatible board and implements layers 1 and 2 of the ISO model for IEEE 802.3 (Ethernet) LANs. Based on the 82586 LAN coprocessor chip, the board can run the vendor's iNA 960 ISO transport- and network-layer software. You can also use the vendor's iRMX-Net software to implement layers 3 through 7 of the ISO protocols, enabling concurrent file sharing by systems using the iRMX operating system. $600 (100).

Intel Corp, Literature Dept W-272, 3065 Bowers Ave, Santa Clara, CA 95051. Phone (408) 986-8674.

Circle No 392



MEMORY BOARDS

The Model 1501 VME Bus memory board is available in 150- and 200-nsec access-time versions and with either 1M or 2M bytes of dynamic RAM. Designed to the VME, Revision C, specification, the boards implement test and set instructions.

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CIRCLE NO 171

Houston Instrument's new E size DMP-56 delivers the precision, throughput, and reliability you require from a drafting-intensive plotter. The DMP-56 also gives you the flexibility to handle 18 different drawing format sizes ranging from 8½ × 11 inches to 36 × 48 inches.

The DMP-56 was designed for any application calling for crisp, clean graphics—whether it's architectural floorplans, mechanical designs, electrical schematics, or overhead transparencies. Because of its media-size adjustment mechanism and automatic media-size sensing feature, the DMP-56 quickly and efficiently responds to your changing format requirements. This high-performance plotter can produce standard (A through E), metric (A4 through A0), oversize (A4 through A0), and Architectural C, D, and E drawings.

The DMP-56 is a professional drafting plotter that draws on the established track record of Houston Instrument's very successful DMP-51/52 and DMP-51/52 MP plotters—plotters that redefined the standard for price, performance, and quality.

Immediately compatible with hundreds of computer-aided design and graphics software packages through our powerful DM/PL™ command language, the DMP-56 also gives you a precise resolution of .001 inch and a maximum plotting speed of 17 inches per second. And, because it uses a standard RS-232-C compatible interface, the DMP-56 can operate with virtually any computer on the market.

The DMP-56 also delivers features you'd expect only from more expensive* plotters—such as quiet servo drive, and an easy-to-use front-panel control. Combine these standard features with the well-known Houston Instrument reliability and support and you have a superior plotter at a reasonable price.

In terms of throughput, performance, price, and quality the DMP-56 is the professional graphics tool you need. For more information, call 1-800-531-5205 (512-835-0900 if in Texas), or write Houston Instrument, 8500 Cameron Road, Austin, Texas 78753. In Europe, contact Houston Instrument, Belgium NV., Rochesterlaan 6, 8240 Gistel, Belgium. Tel.: 32-(0)59-277445. Tlx.: 846-81399.

*U.S. suggested retail price is $5,995. Pricing subject to change.
DM/PL is a trademark of Houston Instrument.

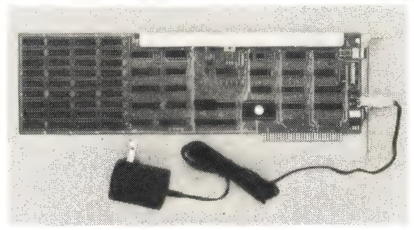
houston instrument
A Division of AMETEK

CIRCLE NO 172

They are compatible with address-pipelining bus masters, and end users can program the address multiplier decoder. The 200-nsec version costs $800 and $1295 and the 150-nsec version costs $1000 and $1695 for 1M byte and 2M bytes of RAM, respectively. Delivery, stock to 45 days ARO.

Computer Products, Grant Technology Div, 11 Summer St, Chelmsford, MA 01824. Phone (617) 256-8881.

Circle No 393



RAM-DISK BOARD

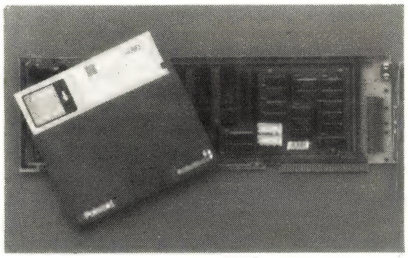
The Novo Drive 1000 board emulates a 1M-byte disk drive when installed in an IBM PC/XT or compatible computer. A standby power module and 2-hour battery backup protect data while your power is out, your PC is off, or you're moving the board from one PC to another. According to the manufacturer, the board accesses data 64 times faster than a floppy disk, 30 times faster than a hard disk, and twice as fast as a virtual disk in the PC's memory. Onboard firmware can boot the system from the card, and you don't need special drivers or programs to access the card. $395.

Kapak Design, 18784 Cox Ave, Saratoga, CA 95070. Phone (408) 378-4444.

Circle No 394

SERIAL I/O BOARD

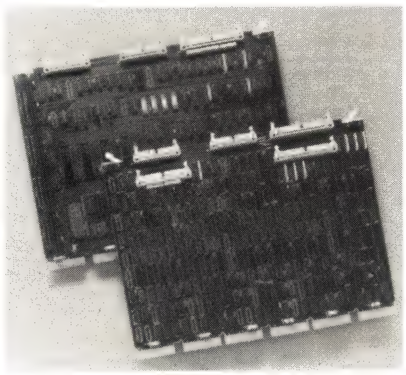
The Multi-User board provides eight serial ports for the IBM PC/XT, PC/AT, and compatible computers. It functions as an interrupt-driven I/O device and provides the control lines necessary to drive most asynchronous terminals, print-



ers, and modems. To install it, you plug it into an expansion slot and route two 36-pin ribbon cables through the back of the PC to a terminal box. The terminal box contains eight 25-pin RS-232C ports. A software device driver, operating under Xenix on the PC/AT, controls as many as eight terminals through the board. On the PC/XT, you address the ports as COM1 through COM8 under DOS. $575; 4-port model, $375.

American Micronics Inc, 17811 Skypark Circle, Suite H, Irvine, CA 92714. Phone (714) 261-2428. TLX 314016.

Circle No 395



Q BUS DISK DRIVES

The Concept 15 subsystem for Q Bus computers can transfer data at rates as high as 9.3M bytes/sec. At that rate, the subsystem can implement real-time image processing; eg, it can refresh a 512×512-pixel image 30 times/sec. The M2350A parallel-transfer disk (PTD) drive from Fujitsu makes possible the peak transfer rate. The subsystem can control and format either one or two PTD drives. It includes the RMO2 software interface for the Q

Bus and automatic chaining of I/O operations. The two boards in the subsystem measure 15.7×12 in. and cost $14,100; the subsystem plus one PTD drive costs $41,000. Delivery, 60 days ARO.

Storage Concepts Inc, 3198-G Airport Loop Dr, Costa Mesa, CA 92626. Phone (714) 557-1862.

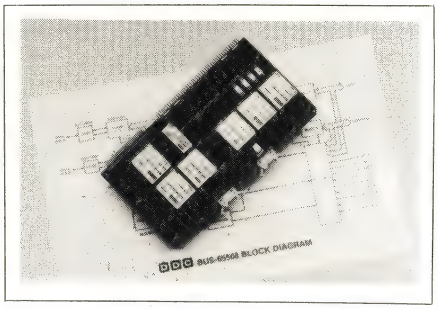
Circle No 396

PC ACCELERATOR

RaceCard-286, a plug-in card for the IBM PC, runs software as much as six times faster than the PC's 8088 μP. Measuring 5×3.9 in., it fits into a short slot on the computer. The card's 80286 μP emulates the IBM 8088 native processor; if you need greater numeric processing, you can insert an 80287 floating-point coprocessor. You install the card by placing it into any short slot, removing the 8088 on the PC's motherboard, and then running a jumper from the RaceCard-286 to the open socket. The card consumes 7W from the PC's power supply. $795.

Mountain Computer Inc, 360 El Pueblo Rd, Scotts Valley, CA 95066. Phone (800) 458-0300; in CA, (800) 821-6066. TWX 910-598-4504.

Circle No 397



1553 INTERFACE

The BUS-65508 Multibus interface card connects the Multibus and the MIL-STD-1553 serial-mux data bus. The 6.75×12-in. card includes a 4k×16-bit memory, six subsystem command registers, and four types of subsystem interrupts. Fully compliant with MIL-STD-1553, the card supports all message formats, implements 12 mode codes, and provides built-in test capability. The card can serve as any one of four devices on the Multibus. As a bus-slave device, it acts as a programmed I/O device to the bus's host processor; as a bus controller, it can store and process as many as 62 messages of 64 words each without subsystem intervention. As a remote-terminal unit, the card can store and respond to as many as 119 messages of 32 words each without subsystem intervention, and as a bus monitor, it can keep track of all activity on the 1553 data bus. $7695. Delivery, stock to eight weeks ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 510-228-7324.

Circle No 398

Microsoft FORTRAN. The overwhelming favorite.

How did Microsoft® FORTRAN get so popular?

It could be the mainframe compatibility. Our compiler makes porting applications a cinch with overlays and the ANSI features you need.

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It could be the XENIX® and MS-DOS® source-level compatibility. Or the direct inter-language calling to Microsoft C, Pascal and Assembler. Or the ability to work with our Macro Assembler's symbolic debugger.

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Why is Microsoft FORTRAN the most popular FORTRAN?

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Microsoft FORTRAN Compiler Version 3.3 for MS-DOS and XENIX 286

Microsoft FORTRAN Compiler
- Implements most ANSI 77 standard features, plus extensions.
- Easily port mainframe/minicomputer programs with little or no modification.
- Overlay support in the compiler and linker.
- Common blocks and arrays greater than 64K.
- Supported by the largest number of third party libraries.
- Includes a full set of math libraries to select from:
  - 8087/80287 emulation.
  - 8087/80287 coprocessor support.
  - Floating Point without 8087/80287.
  - BCD Floating Point.
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- Simple overlay linker combines relocatable object modules created using Microsoft languages into a single program.
- Link very large programs (over 1 megabyte) using overlays.

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- A utility to pack EXE files for smaller size on disk and faster loading at execution time.

Microsoft EXE File Header Utility (MS-DOS only)
- A utility that allows you to display and modify the fields in EXE file headers.

For the name of your nearest Microsoft dealer call (800) 426-9400. In Washington State and Alaska, (206) 828-8088. In Canada, call (800) 387-6616.

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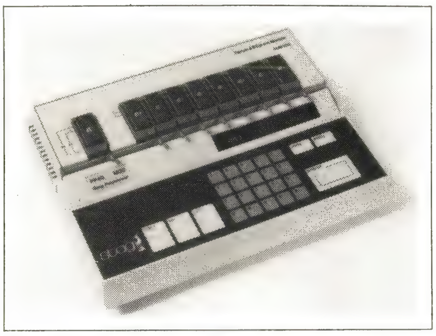


EPROM PROGRAMMER

The Model PP40 programs most EPROMs and EEPROMs, handling as many as eight devices simultaneously and using device manufacturer's fast programming algorithms. The system has an integral 16-character alphanumeric display and a 16-key hexadecimal keyboard. Bicolored LEDs indicate status and report error conditions at each of the sockets. Plug-in modules handle different device types and package styles, including leadless chip carriers. You can update the software. $1495.

Stag Microsystems Inc, 528-5 Weddell Dr, Sunnyvale, CA 94089. Phone (408) 745-1991. TWX 910-339-9607.

Circle No 413

STD FORTH

A development system based on Forth Inc's PolyFORTH real-time multitasking OS and programming language is available for this manufacturer's ZT 8806/8807 computers. The development system includes the 8088-based ZT 8806 (with PolyFORTH in PROM), the ZT 8820 byte-wide memory board, a 3½-in. floppy disk and controller, a card cage, and a power supply. The software system includes Forth, an 8086/88 assembler, an editor, database support, utilities, and a math package for the 8087 coprocessor. The ZT 8806 single-board computer features a 5- or 8-MHz 8088 CPU and supports as much as 192k bytes of PROM and 64k bytes of RAM. You can add an 8087 numeric data processor. Development system, $1995; software, $600 to $3200; ZT 8806, $395.

Ziatech Corp, 3433 Roberto Ct, San Luis Obispo, CA 93401. Phone (805) 541-0488. TLX 4992316.

Circle No 414

DATA SYSTEM

The Megadac 2210C data-acquisition system captures and records analog data at rates to 20,000 samples/sec with 12-, 14-, or 16-bit resolution. You can power the device with a 12V dc, 7A source because it does not require a dc/ac inverter. The device has an RS-232C interface; an IEEE-488 interface is optional. Features also include preprocessing and postprocessing firmware, as many as 128 differential input channels, as much as 60M bytes of real-time mass storage, and direct connection to low-level transducers. $14,900.

Optim Electronics Corp, Middlebrook Technology Park, 12401 Middlebrook Rd, Germantown, MD 20874. Phone (301) 428-7200.

Circle No 415

DC/DC CONVERTERS

The DCA, DCB, and DCC family of isolated dc/dc converters includes 64 models of single-, dual-, and triple-output units with power capabilities of 15 to 30W. Efficiency is 80% min and calculated MTBF (to MIL-STD-217D) is as high as 400,000 hours. Outputs of 5, 12, 15, 24, ±12, ±15, 5 and ±12, and 5 and ±15V are standard. All models are available in four input ranges of 9.2 to 16V dc (12V nominal), 19.2 to 31.2V dc (24V nominal), 38.4 to 62.4V dc

BOURNS

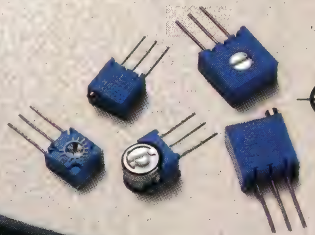
Now you can extend the cost saving advantages of your automated component insertion process to include Trimpot® trimming potentiometers, the industry's most popular.

Bourns Trimpot's unmatched selection on tape and reel provides a choice of five models in nine pin configurations to fit almost any application. Top or side adjust in round or square packages and 1/4'' or 3/8'' make for easy PC board placement and maximum design flexibility.

Bourns' tape and reel packaging is compatible with all major radial insertion equipment on the market and meets EIA standard RS-468. Every model also reflects the high quality design and manufacturing standards you expect from Bourns.

So, when you're ready to automate trimmer placement, do it with the extraordinary confidence of Bourns Trimpot experience, worldwide availability and service. There's still no equivalent.

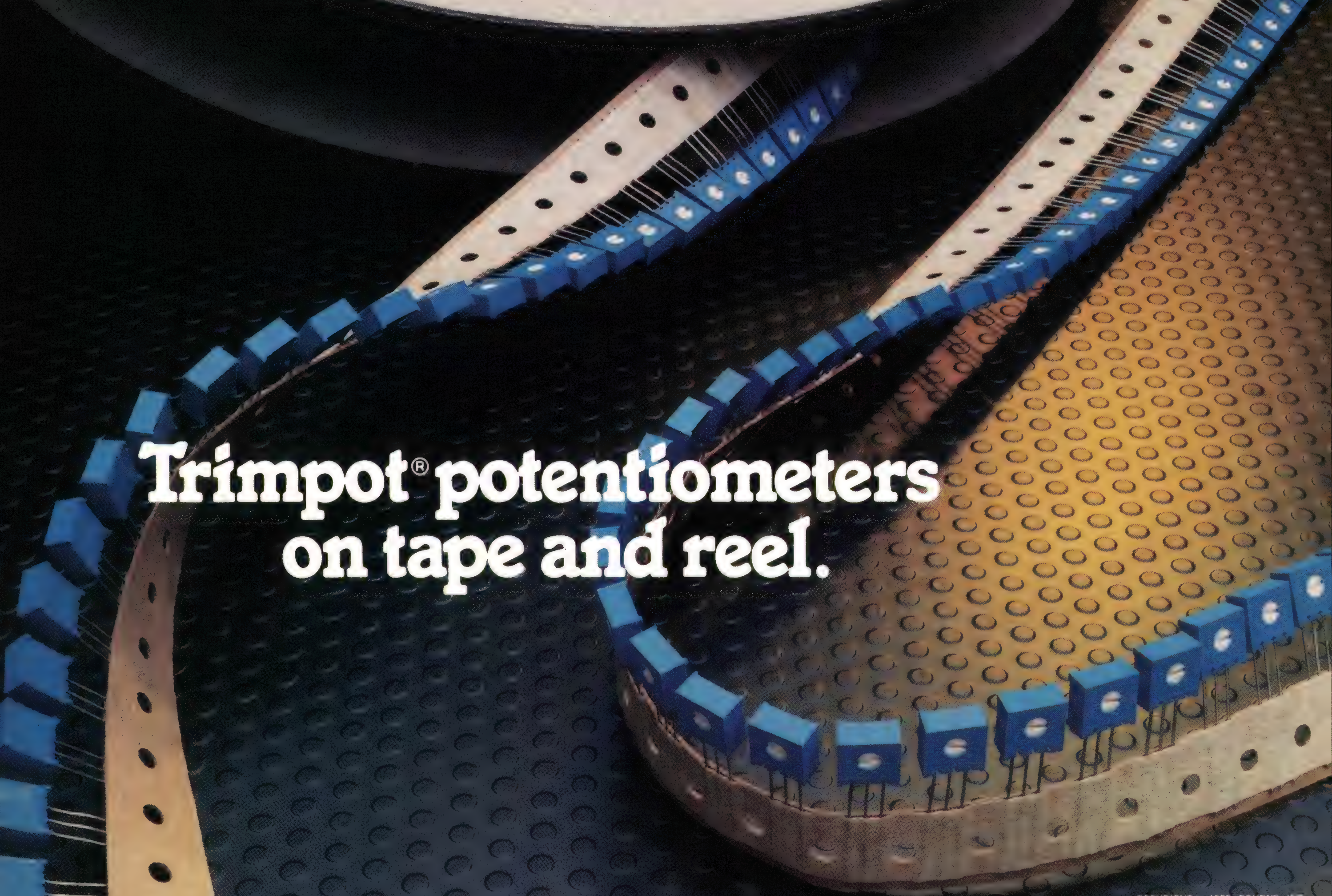
Write for our new catalog on tape and reel models today. Bourns Trimpot, 1200 Columbia Avenue, Riverside, CA 92507. (714) 781-5050.



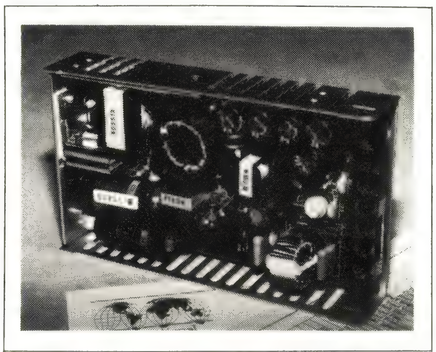
BOURNS®

BOURNS TRIMPOT

CIRCLE NO 175



Trimpot® potentiometers on tape and reel.



(48V nominal), and 85 to 140V dc (110V nominal). These convection-cooled units are packaged in closed metal cases ranging from 1.0× 4.6 × 3.2 in. to 1.3 × 6.3 × 3.2 in. and are specified at full rated load from 0 to 50°C. Features include isolated and adjustable outputs, foldback current limiting, overvoltage clamping, a π-input filter and reverse-polarity protection. $59 to $109. Delivery, stock to six weeks ARO.

International Power Sources Inc, 81 Speen St, Natick, MA 01760. Phone (617) 651-1818.

Circle No 416

MICRO-OHMMETER

In addition to providing 10-μΩ sensitivity, the Model 580 micro-ohmmeter has the ability to clamp the output voltage to 20 mV for dry-circuit applications, to select both test-current polarity (positive or negative) and test-current mode (pulsed or dc), and to automate measurements via an optional IEEE-488 interface. The unit comes with three sets of 4-wire test leads (and a pouch in which to house them), and it has an optional battery pack for applications requiring portable operation. The micro-ohmmeter has a measurement range of 10 μΩ to 200 kΩ. Other features include a 4½-digit display with annunciators, continuous or single-trigger operating mode, and digital calibration. $1495.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (216) 248-0400. TLX 985469.

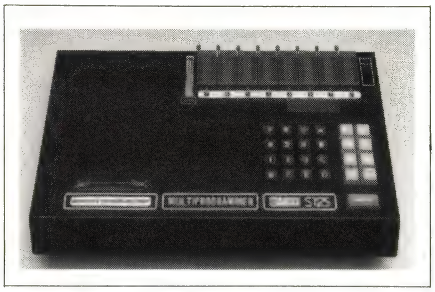
Circle No 417

DC/DC CONVERTER

The DCC dc/dc converter provides 40W in a triple-output configuration. The open-frame converter measures 3.94×6.3×1.35 in. (standard Eurocard dimensions). It has an input range of 3.5:1 (10 to 35V dc and 20 to 70V dc). Available output voltages are 5 and ±12V and 5 and ±15V. This isolated converter features an adjustable primary output (4.9 to 5.4V dc), isolation to 1500V dc, overvoltage protection, short-circuit protection, and soft start. $202.

Intronics Inc, 57 Chapel St, Newton, MA 02158. Phone (617) 964-4000. TWX 710-335-6835.

Circle No 418



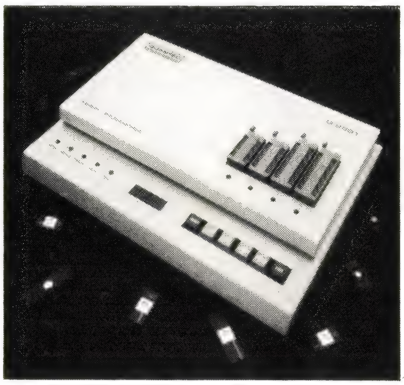
PROGRAMMER

The S125 multiprogrammer programs over 800 devices, including NMOS- and CMOS-based EE-PROMs, bipolar PROMs, single-chip μCs, and various PLDs. The basic system accommodates MOS-processed ICs without the need for additional modules or personality adapters. By using optional modules, the programmer provides support for other PLDs, such as bipolar PLAs and PROMs. All programming is software controlled and uses the industry's fastest algorithms,

according to the manufacturer. The programmer comes with a 25-key, full-travel keyboard and a 16-character×2-line LCD. It offers variable-word-length gang programming; the ability to program 8-, 16-, 32-, and 64-bit words in one operation; and expandable internal RAM (64k to 16M bits). Two serial RS-232C ports and a parallel printer port are available. $995.

Bytek Corp, Instrument Systems Div, 1021 S Rogers Circle, Boca Raton, FL 33431. Phone (305) 994-3520.

Circle No 419

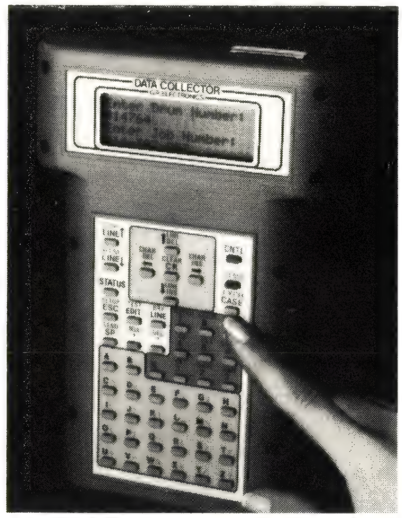


PLD PROGRAMMER

The Q2000 base unit contains the hardware and power supplies necessary to accommodate various types of programmable-logic devices via a choice of plug-in family modules. The programmer reads electronic identifier codes of silicon signatures, which automatically select the correct programming parameters for a particular device. An EPROM-programming module is available now, and future modules will support programmable-logic devices such as PALs, FPLAs, PLAs, and IFLs; bipolar PROMs; and VLSI fuse-logic devices and custom parts. Measuring 3.25×9.25×13.5 in., the Q2000 weighs approximately 16 lbs. Q2000 base unit, $1495; family modules begin at $595.

Destron Technologies Inc, 385 Elliot St, Newton, MA 02164. Phone (617) 332-4621.

Circle No 420

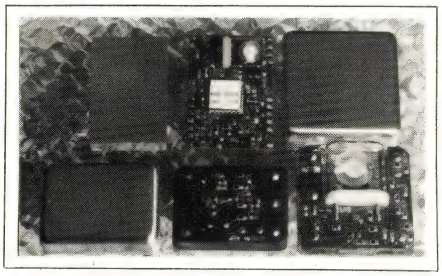


HANDHELD TERMINAL

The 84C handheld data collector offers 8k, 32k, 64k, or 256k bytes of battery-backed memory and a 4-line×20-character display. The terminal uses a form of integer Basic. You can write, edit, list, and run programs entirely on board, or you can write them as source on any external computer and then download them. The user configures the assignment of key functions. The data collector can transmit, receive, and display the ASCII 128-character set, including control codes. With the aid of the optional bar-code reader, it can read the most frequently used bar codes. A choice of interfaces includes RS-232C, RS-422, or 20-mA current loop at baud rates as high as 19,200 bps. Handshaking for RTS/CTS/DTR is standard, as is a real-time clock. NiCd batteries provide as much as 50 hours of continuous use. 8k-byte model, $1065; 32k-byte model, $1295; 64k-byte model, $1495; 256k-byte model, $2245.

GR Electronics, 1640 Fifth St, Santa Monica, CA 90401. Phone (213) 395-4774.

Circle No 421



SAW DEVICES

Three new surface acoustic wave (SAW) devices include a resonator filter, a low-loss transversal filter, and SAW oscillators. Housed in a TO-39 package, the resonator filter is available with a 400- to 800-MHz frequency range. Its bandwidth ranges from 0.05% to 0.2% of center frequency. The frequency range can be extended down to 100 MHz or up to 1.2 GHz. The resonator filter specs an insertion loss of 4 dB. The low-loss transversal filter covers a 150- to 678-MHz frequency range and has a bandwidth of between 0.2% and 0.5%. It specs an insertion loss of <6 dB. The SAW oscillators cover a 100-MHz to 1.2-GHz frequency range and offer an uncompensated stability of 100 ppm over −40 to +85°C. From £100 (100).

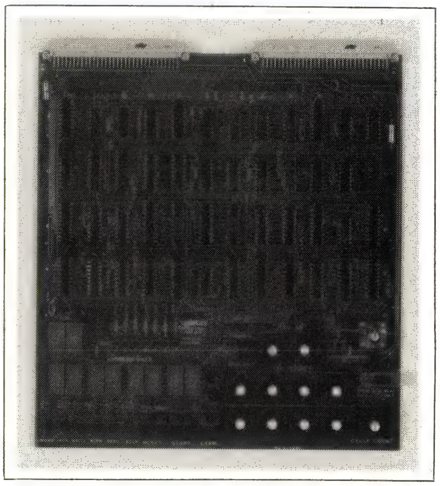
STC Components Ltd, Quartz Crystal Unit, Edinburgh Way, Harlow, Essex CM20 2DD, UK. Phone (0279) 26811. TLX 818746.

Circle No 399

Stantel Components, 636 Remington Rd, Schaumberg, IL 60195. Phone (312) 490-7150.

Circle No 400

VME-BUS ANALYZER



Using the PG2800 analyzer module, you can trace program flow or carry out hardware troubleshooting on VME Bus computer systems. The module captures specific bus cycles and displays the bus address or data information as well as the condition of associated bus signal lines. The address, address modifiers, and data-bus information are displayed as 7-segment hexadecimal characters; individual LEDs display the conditions of other relevant bus lines. The extended double Eurocard module plugs directly into the VME Bus backplane. A pushbutton that generates a VME Bus Sysreset* signal is also provided. $995.

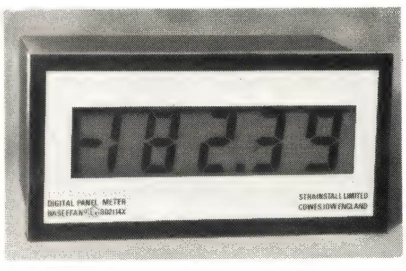
Philips, Industrial & Electro-Acoustic Div, Box 523, 5600 AM

Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 401

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 991-2000.

Circle No 402



PANEL METER

The D9400 digital panel meter has Baseefa and Cenelec safety certification, suiting it for use in hazardous industrial environments. The meter features a 4½-digit, 1-in.-high LCD with polarity indicators and a jumper-selectable decimal-point position. It's housed in a standard DIN enclosure with front-panel bezel dimensions of 144×72 mm. It has two input-voltage ranges of 0 to 200 mV and 0 to 2V, and a current-input range of 4 to 20 mA. Measurement accuracy is ±0.01%±2 digits and maximum linearity error is 3 digits. You can introduce an internal attenuator into the input circuitry, which allows you to vary the input attenuation between 1:1 and 6:1. With the attenuator in the circuit, input impedance on the voltage ranges is reduced to 60 kΩ. The meter samples the input at 1.67 readings/sec. £364.

Strainstall Ltd, Cowes, Isle-of-Wight PO31 7TB, UK. Phone (0983) 295111. TLX 86369.

Circle No 403

POWER-SUPPLY TESTER

The Powerload 50 electronic load allows you to test power supplies with either a constant resistance load or a constant current load as high as 10A. The unit has a maximum continuous load dissipation of 50W and an input-voltage capability of 3 to 75V. You set the load value via a multiturn rotary control, and the unit has a built-in digital panel meter to indicate the load current on 2A and 20A scales. You can remotely program current loads using a 0 to 10V programming input and remotely monitor the current on a 100-mV/A monitor output. The load operates over 0 to 40°C and has automatic overtemperature protection. It may be powered from internal rechargeable batteries to avoid common-mode problems in the load circuit. The unit measures 132×135×220 mm. Approximately Sw Kr 2500.

Powerbox AB, Box 148, 154 00 Gnesta, Sweden. Phone (0158) 11920. TLX 11502.

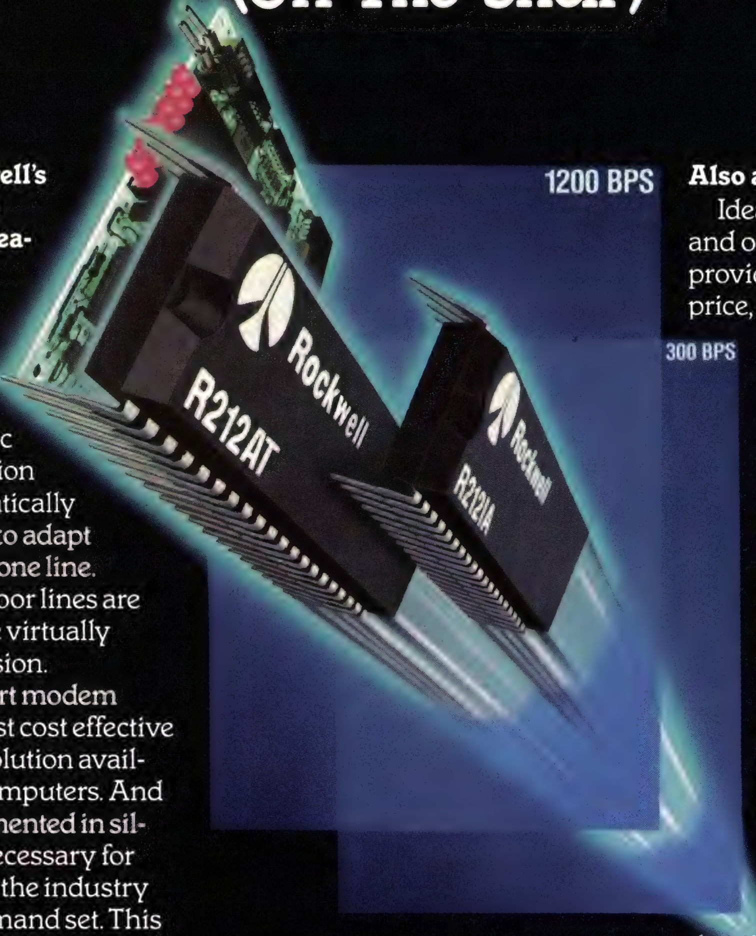
Circle No 404

LOGIC ANALYZER

The D1201 logic analyzer provides 32- or 48-channel state analysis and 16-channel timing analysis at clock rates to 200 MHz. Trigger facilities include sequential triggers at as many as 16 levels or 8-level selective

ROCKWELL SEMICONDUCTOR TECHNOLOGY DELIVERS 1200 BPS AT 300 BPS PRICES.

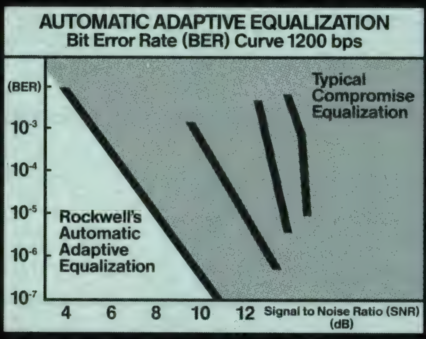
(Off-The-Shelf)



Introducing Rockwell's new R212AT smart modem device set featuring Automatic Adaptive Equalization.

Rockwell International's exclusive Automatic Adaptive Equalization Algorithms automatically enable the modem to adapt to any quality of phone line. Even signals over poor lines are enhanced to ensure virtually error-free transmission.

The R212AT smart modem device set is the most cost effective communications solution available for personal computers. And R212AT has implemented in silicon the software necessary for compatability with the industry standard "AT" command set. This allows quick design-in because we've presolved all the "AT" dialing functions. It incorporates auto dial, auto answer and can dial DTMF tones or pulses.



The R212AT smart modem offers lower system cost because it incorporates the controller and analog filter circuitry required for modem communications in the device set itself. This reduces parts count, enhances total system reliability and meets low power requirements for portable applications.

As well as operating asynchronously, the R212AT has synchronous mode operation for higher transmission throughput.

Also available: Rockwell's R212DP.

Ideal for remote diagnostics and other integral applications, it provides specific advantages in price, performance and system cost savings.

The R212DP, like the R212AT, has automatic fall back to slower speeds and an RS232C interface. Both these Bell 212A and 103 compatible device sets are available at any level of integration from devices to boards or customized private label systems.

For ease of evaluation, Rockwell provides a board level evaluation modem for laboratory analysis to assure the performance and quality of R212AT and R212DP.

Call your local Rockwell distributor today for off-the-shelf delivery of an evaluation board complete with a Designer's Guide Kit.

Semiconductor Products Division
Rockwell International, P.O. Box C,
M.S. 501-300, Newport Beach,
CA 92658-8902 (800) 854-8099.
In California (800) 422-4230.

Rockwell International

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Aerospace / Electronics / Automotive
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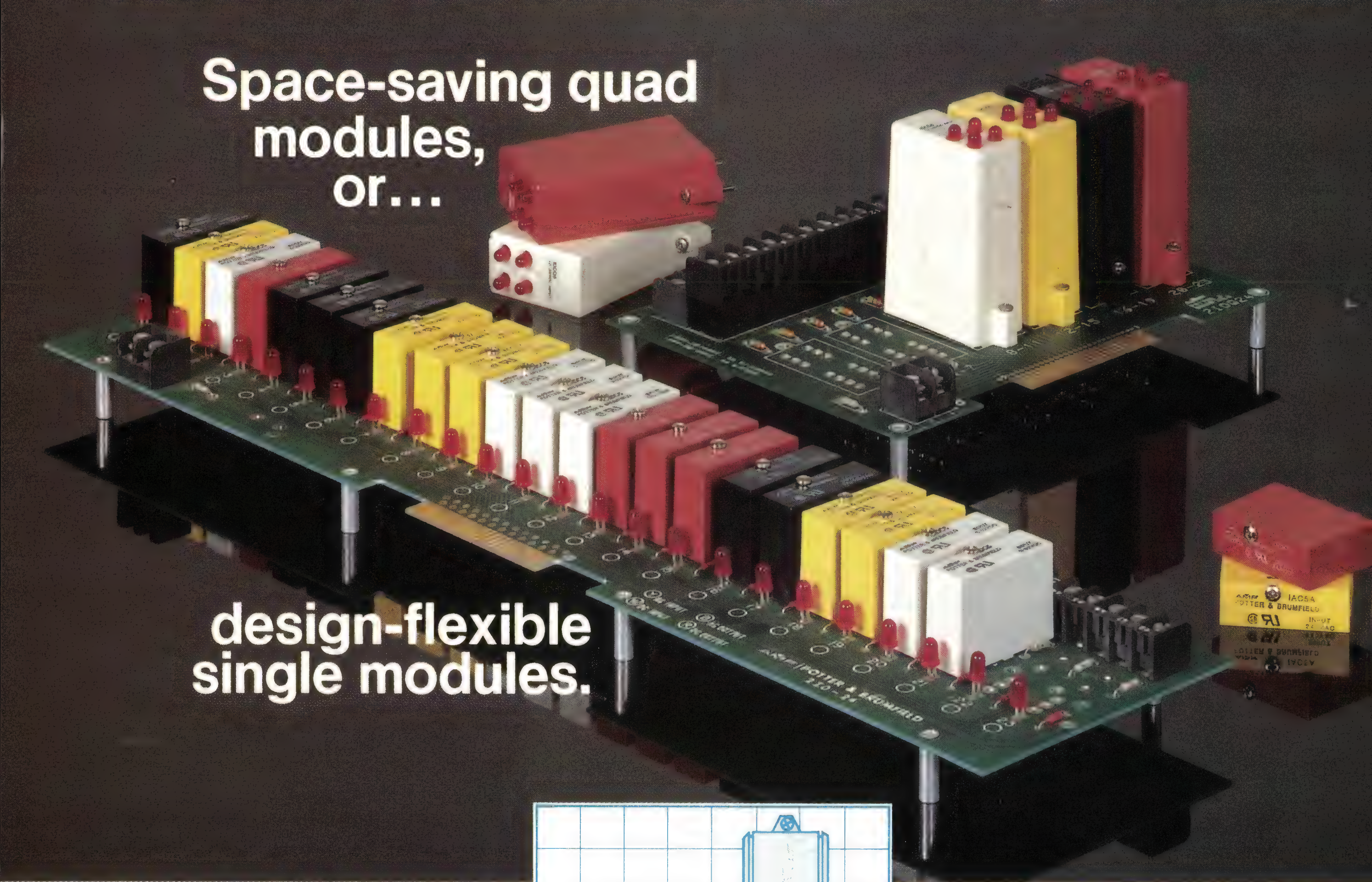
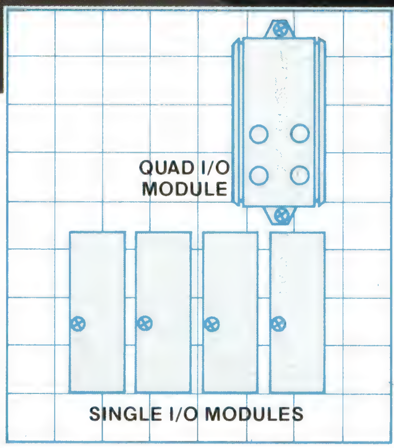
CIRCLE NO 177

P&B offers you the I/O options you need!

Space-saving quad modules, or…



design-flexible single modules.



P&B's compact, quad input/output modules are perfect for your industrial control applications with limited space available for interface devices. Each quad module has four I/O channels in a single, plug-in package. An LED indicator is provided for each channel, and modules are color-coded by function.

For designs requiring even more flexibility, our single I/O modules provide single channel pluggability in four photo-isolated, color-coded versions.

Both types reliably interface microprocessor- or computer-based systems with "real world" input devices and loads. Models for use with 5, 15, and 24 volt DC logic systems are in stock. And they have advanced features which many competitors' units lack.

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Find out more about P&B I/O products. For the name of your nearest authorized stocking distributor or sales representative, call toll-free **800/255-2550**. Potter & Brumfield, 200 S. Richland Creek Drive, Princeton, IN 47671-0001.

Regional Sales: Oak Brook, IL, 312/887-0811; Braintree, MA, 617/848-6550; San Juan Capistrano, CA, 714/493-4503; Norcross, GA, 404/449-4601.
International Sales: Guelph, Ontario, 519/822-1576, TELEX: 0695-6522; Bristol, England, (0272) 716301; Yokohama, Japan, (045) 812-1418; Hong Kong, TELEX: 39555; Chatswood, N.S.W. Australia, (02) 411-5222; Taipei, Taiwan, (02) 700-2923/4.

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CIRCLE NO 178

triggering. An additional module provides a disk drive and CP/M operating system for computing functions, including IEEE-488 controller functions. Other options include a 50-MHz-sampling-rate waveform recorder and counter/timer and signature-analysis modules. DM 25,000 to DM 47,000.

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 405

OSCILLOSCOPE

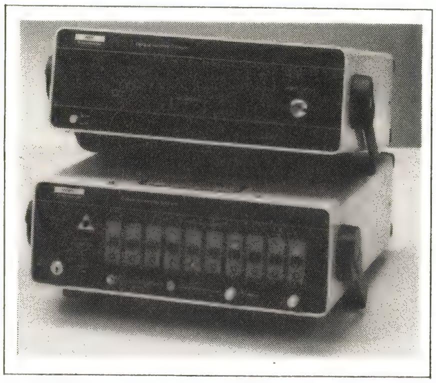
The PM3295 is a 350-MHz, 2-channel, dual-time-base portable oscilloscope with full manual and IEEE-488 bus control. The μP-controlled scope has an intelligent autoset/beamfinder function, which automatically provides initial channel gain and time-base ranges for the display. The scope's vertical-input sensitivity ranges from 1 mV/div to 5V/div; you can switch the input impedance between 50Ω and 1 MΩ. Internal and external trigger facilities are provided. The main and delayed time bases provide sweep rates from 1 nsec/div to 10 sec/div. On-screen voltage and time cursors and alphanumeric screen readouts allow you to make measurements on displayed waveforms. The IEEE-488 interface allows you to enable selectively one or more front-panel controls for interactive test setups; battery-backed memory lets you store front-panel setups during power-down periods. The oscilloscope operates from a 90 to 260V ac line supply and is tested to MIL-28800C specs. With IEEE-488 interface, $5950; without interface, $5150.

Philips, Industrial & Electro-acoustic Systems Div, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 406

Philips Test & Measurement Inc, 85 McKee Dr, Mahwah, NJ 07430. Phone (201) 529-3800.

Circle No 407



FIBER-OPTIC TESTER

Combining the Model 7730 optical transmitter and the Model 7731 optical receiver, you can measure the bandwidths of 50/125-μm multimode optical fibers at a wavelength of 840 nm. The transmitter has a 1.8-mW laser source, which you can amplitude-modulate from one of 10 internal frequency sources in the 5- to 250-MHz range. You can also modulate externally at frequencies as high as 1 GHz. The receiver detects and demodulates the fiber's optical output, providing a signal suitable for display on a spectrum analyzer or high-frequency power meter. The receiver has an optical dynamic range of approximately 50 dB; operating frequency ranges from 1 MHz to 1 GHz. To perform bandwidth measurements, you first couple the two instruments via a short-fiber link and adjust the amplitude of each frequency source to give the same received power at the receiver. Using the fiber under test, you then sweep through the frequencies, noting the attenuation at each frequency to measure the fiber's spectral response and hence its bandwidth. You can select frequen-

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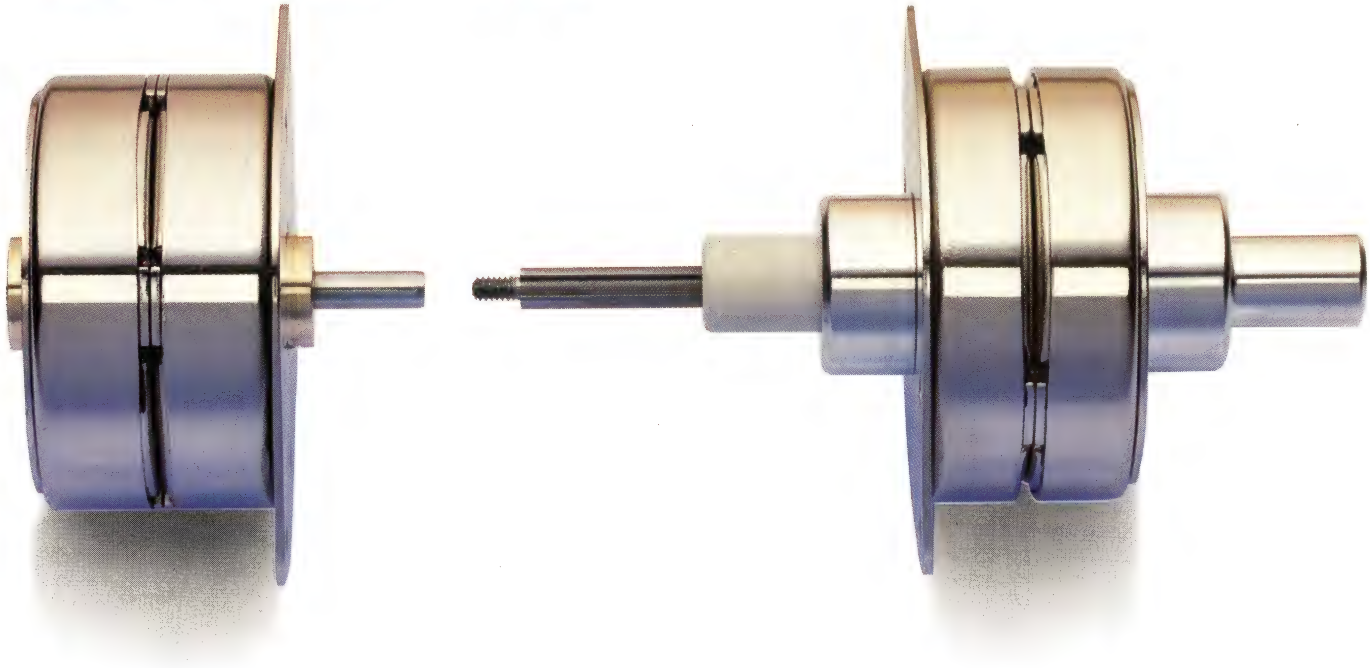

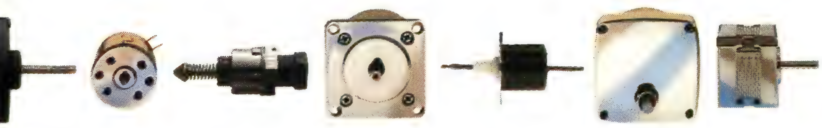

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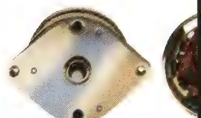

cies manually or via the transmitter's 0.6- to 1.4-sec/sweep internal-sweep function. Model 7730, Fr fr 98,500; 7731, Fr fr 47,850.

Enertec-Schlumberger, 5 rue Daguerre, 42030 St Etienne Cedex 2, France. Phone (77) 252264. TLX 300796.

Circle No 408

LED DISPLAYS

Suited for use in military and avionic environments, the GPD-474 and GPD-474P 4½-digit, 7-segment LED displays feature hermetically sealed ceramic cavity packages and visibility in sunlight. Both displays have 4-mm-high characters. The -474P version also features contrast enhancement achieved by a black chroming process used in the manufacture of the LEDs. GPD-474, £115; -474P, £125 (100). Delivery, 10 weeks ARO.

Plessey Optoelectronics Ltd, Wood Burcote Way, Towcester, Northants NN12 7JS, UK. Phone (0327) 51871. TLX 312428

Circle No 409

Plessey Solid State, 3 Whatney Ave, Irvine, CA 92718. Phone (714) 951-5212.

Circle No 410

RELAY

Measuring 32.2×27.9×27.4 mm, the AZ-2100 miniature heavy-duty relay can switch a maximum of 720W/5500 VA at a maximum switching voltage of 60V dc or 280V ac and a maximum load current of 30A. The relay is available with a choice of one NO, one NC, or one change-over contact, and with nominal coil voltage ratings between 5 and 48V dc. Its mechanical lifetime is 10M switching operations. The relays meet VDE group C insulation requirements and are tested to 2.5 kV rms between coil and contacts. Contact connections are via push-fit connectors on the upper side; coil connections are via solder connectors on the lower side. The relay housing, providing protection to IP 67 DIN 40050 standards, accommodates automatic soldering and solvent cleaning processes. Less than DM 6 (10,000).

Zettler GmbH, Holzstr 28-30, 8000 Munich 5, West Germany. Phone (089) 23881. TLX 523441.

Circle No 411

AUDIO TEST SET

The MJS401D audio measuring system measures signal level, noise, frequency, distortion, and crosstalk. Plug-in options include additional A-weighting and CCITT-weighting filters; a module for intermodulation distortion measurement to SMPTE, DIN, and CCIF standards; and a wow and flutter meter. The standard unit incorporates a twin-tone precision oscillator. Level measurement range extends from −110 to +40 dBm, and accuracy is better than 0.1 dB. You can make distortion measurements to a level of 0.0008% (−102 dB). The level meter automatically switches from ±12 to ±1.5 dB to accommodate equipment adjustment. You can set the reference level with a resolution of 1 dB on the instrument's front panel. An IEEE-488 interface is optional. Approximately $5100. Delivery, four to six weeks ARO.

Technical Projects Ltd, Unit 2, Samuel White's Industrial Estate, Medina Rd, Cowes, Isle of Wight PO31 7LP, UK. Phone (0983) 291553. TLX 869335.

Circle No 412

PC GRAPHICS

Micro-Speakeasy, which features interactive graphics, a report-writing capability, and approximately 1000 high-level operations, is the latest version of the company's Speakeasy mainframe software. Suitable for PC/MS-DOS environments, the package also comes with Grapheasy, a modular tool kit that produces pie charts, bar charts, line plots with arbitrary complexity of hatching, and shading for drawn figures. To use Micro-Speakeasy, you need an IBM PC or compatible computer with 640k bytes of memory, an 8087 or 80287 math coprocessor, and approximately 5M bytes of hard-disk space. Yearly rental maintenance arrangement, with updates, $750 per copy.

Speakeasy Computing Corp, 222 W Adams St, Chicago, IL 60606. Phone (312) 346-2745.

Circle No 422

REAL-TIME SIMULATOR

An enhanced version of Tutsim with real-time and analog data-acquisition features allows you to simulate a large and expensive system in order to evaluate a real control circuit or computer. With the addition of these real-time and real-analog features, you can use the program with the Data Translation 2801 Series A/D and D/A converters with no modification; however, source code in assembly language is provided for the I/O drivers so that you can modify them for use with almost any other D/A or A/D converter. The package lets you solve problems by constructing a block-diagram simulation of a proposed system, running the simulation, and analyzing the results. You can mix block diagrams and graphs in the model and display or print the operating characteristics of that model. You can also obtain a numeric listing of the results. Three versions are available: the short form, intended primarily for high-school and college students; the collegiate version, intended for undergraduate instruction in problems of biophysics, ecology, econometrics, and nonlinear differential equations; and the professional version, intended for the analysis of problems in linear and nonlinear servo systems, robotics, thermodynamics, and chemical engineering. Short form, $39.95; collegiate, $109.95; professional, $495.

Applied i, 200 California Ave, Suite 214, Palo Alto, CA 94306. Phone (415) 325-4800.

Circle No 423

SYMBOLIC COMPUTATION

Version 1.5 of the high-level math language SMP is for interactive symbolic computations. You use it to create, manipulate, and solve symbolic design equations exclusively with familiar algebraic operations. This version also generates error-free Fortran source code for SMP-developed problem solutions and algorithms. The Fortran source code can be separately compiled and incorporated into other Fortran programs for further, nonSMP calculations. This version provides enhanced graphics capability. It features more than 100 built-in symbolic functions with a cohesive mathematical syntax; almost 200 additional functions are available for numerical evaluation of the higher transcendental functions. SMP runs on DEC VAX and MicroVAX machines under Unix or VMS; Apollo, Sun, and Ridge computers; and IBM 370s equipped with VM/CMS. Customer license for one full-time user or three part-time users, $12,500.

Inference Corp, SMP Div, 5300 W Century Blvd, Los Angeles, CA 90045. Phone (213) 417-7997.

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DESIGN TOOL

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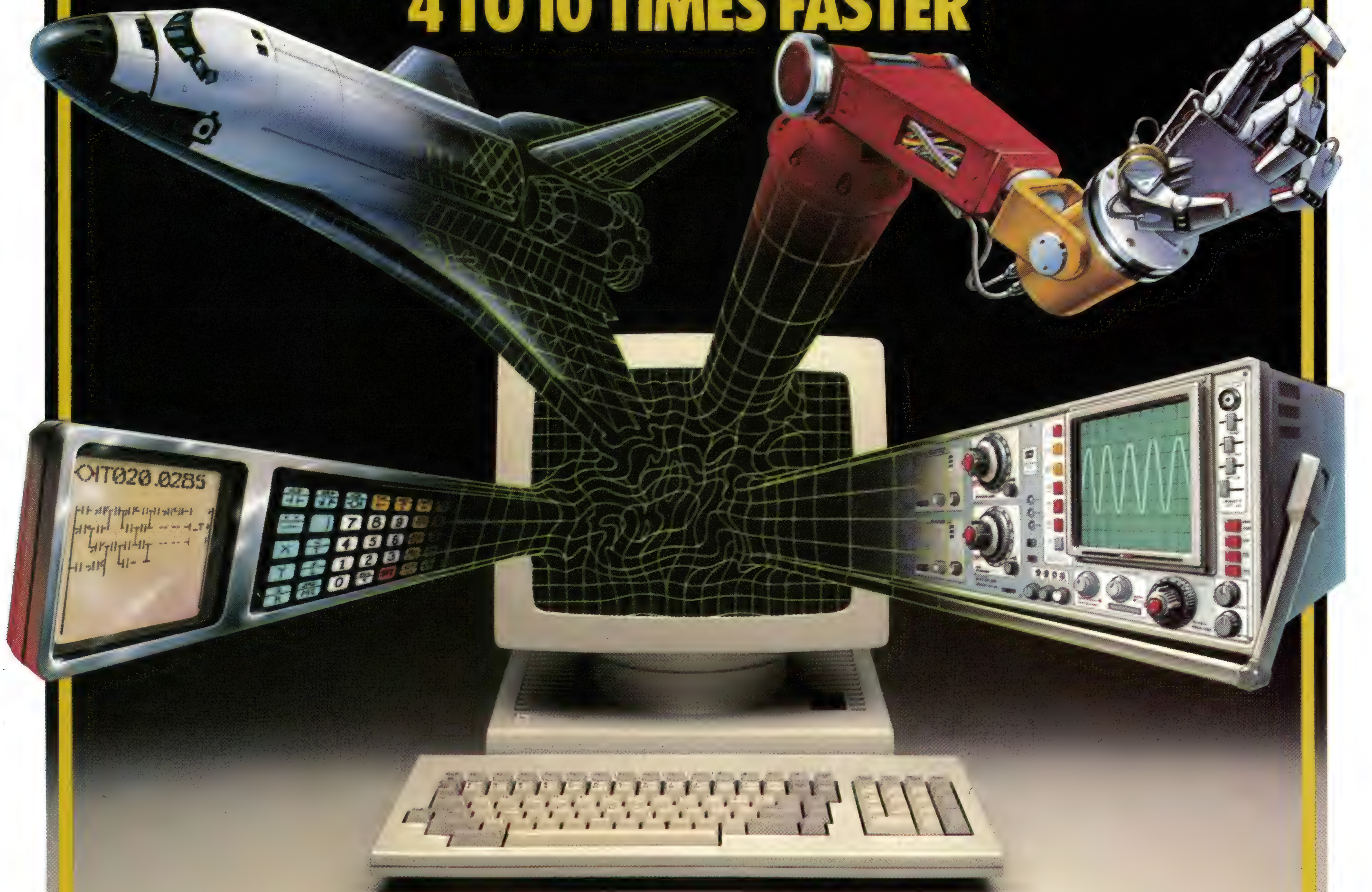

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menting a program or system of programs. The package provides a design language; a processor in software interprets the design statements and generates design documents. Before you write any software code, the software produces design diagrams that communicate your ideas to other designers and to end users. You can use the package for three forms of documentation: language-independent designs of programs and systems, which you can implement in most programming languages; designs to be implemented in Ada; and such documents as reports, reference and users' manuals, and letters. The software runs under MS-DOS. $648.38.

Unidot, 602 Park Point Dr, Golden, CO 80401. Phone (303) 526-9263.

Circle No 425

NETWORK SOFTWARE

This version of Novell's Advanced Netware/O is customized to run on the company's Omninet LAN configured with the Trimline Combo (TLC). The TLC is an add-on disk/tape subsystem for the IBM PC, PC/XT, PC/AT, and compatible computers. The PC/TLC combination runs the network software and can act both as a server unit and as a workstation on the network. The package comes with a library of network applications that are compatible with Novell's file-locking schemes. The package includes the TLC, four Omninet network cards, and the software; it supports eight users and costs $5795. Without the TLC, an 8-user package costs $795; 50-user package, $1595.

Corvus Systems Inc, 2100 Corvus Dr, San Jose, CA 95124. Phone (408) 559-7000.

Circle No 426

SECURITY PACKAGE

Comprising an internal half card, a computer-cover lock, and software, the X-Lock 100 limits access to IBM PCs (or compatibles) and peripherals. According to the company, the lock can't be circumvented because the µP-controlled hardware resides at the BIOS level and is linked to the PC at a subsystem point before the operating system or other software is loaded. You can create as many as 72 user accounts, each with a password. Once you log on, the lock is transparent to software or applications unless you attempt a forbidden activity. The software also monitors the length of time each user is logged on as well as printer use; in addition, it can limit the amount of time a user can access the personal computer. Other features include self-diagnostics, automatic locking after 10 unauthorized attempts to access the system, battery-backed memory, and the ability to accept one-time passwords. $425.

Xtratek Corp, Box 7622, Atlanta, GA 30357. Phone (404) 875-8100.

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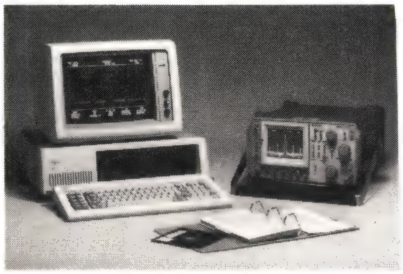

SPECTRUM ANALYSIS

Grasp (general RF applications software package) allows you to make such spectrum-analysis measurements as swept frequency, signal analysis, harmonic distortion, S/N ratio, amplitude modulation, and frequency response. You can store, manipulate, analyze, and compare data; create graphs; and record and plot results. Using a modem, you can check the performance of remote equipment such as satellite communications or radar sites. Three packages are available. S26RF00 options 1 and 1A run on the IBM PC and compatibles that have the company's Guru interface.

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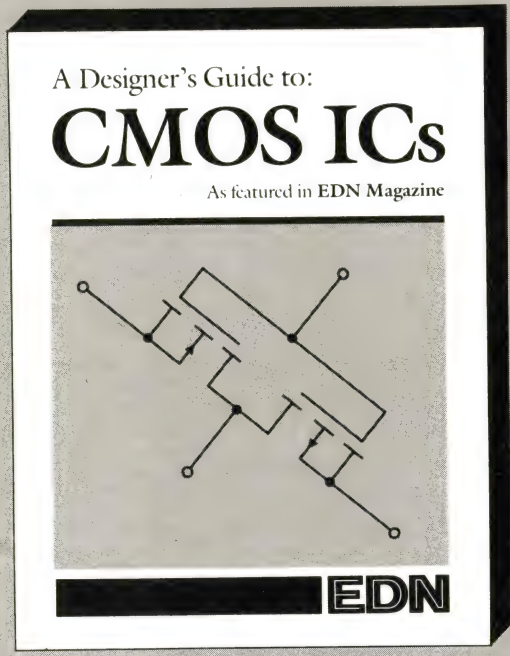

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TURN TO PAGE 320

Options 2 and 2A run on the HP Series 200 controller. Option 3 works with the company's 4105A color graphics terminal and 4041 system controller. $875 each.

Tektronix Inc, Box 1700, Beaverton, OR 97077. Phone (800) 547-1512; in OR, (800) 452-1877.

Circle No 428

APL INTERPRETER

The APL Plus UNX system is an enhanced APL interpreter and application-development system that runs under Xenix on the IBM PC/AT. The package provides partial compilation of APL; full-screen editing for creating, viewing, and editing images simultaneously; concurrent file sharing that allows two or more users to safely update component files simultaneously; an external process interface; and nested arrays that are compatible with IBM's APL2. A communications facility allows users to log onto a remote host computer to transfer data. The system requires 1M byte of memory. $995.

STSC Inc, 2115 E Jefferson St, Rockville, MD 20852. Phone (800) 592-0050; in MD, (301) 984-5123.

Circle No 429

BASIC COMPILER

The MT8087 Basic compiler runs on MS-DOS systems equipped with an 8087 or 80287 coprocessor. The compiler maintains accuracy to 18 decimal digits over a range of 10^{-308} to 10^{+308} and provides trig, log, and exponential functions. Trig functions are computed in approximately 1 msec. You can run as many as 10 Basic programs or tasks concurrently. The compiler can start a task on receipt of a hardware interrupt, permitting all device I/O to be interrupt driven. It can use all hardware-interrupt modes, but it will generate software interrupts automatically if no hardware interrupts exist. You can assign as many as 10 windows to separate tasks or multiple windows to the same task. Code generated by the compiler is stored to disk files and can be executed without the Basic interpreter. $79.95.

Softaid Inc, Box 2412, Columbia, MD 21045. Phone (301) 792-8096.

Circle No 430

GRAPHICS PACKAGE

GSS CGI is a computer-graphics interface for raster and vector graphics that meets the ANSI VDI standard and is therefore device independent. The package allows you to develop applications with pop-up menus, windowing, and high-quality text fonts. It also provides definable cursors and fill patterns. You can use the software with the IBM color-graphics adapter, other IBM peripherals, and input and output devices from Hewlett-Packard, Epson, Okidata, Ricoh, Toshiba, Hercules, Microsoft, and Mouse Systems. The interface provides bitmap management in its device drivers, thereby eliminating the need to develop hardware-dependent, bitmap-management routines in your applications. You can design applications to load the controller software as well as device drivers at run time; you can also make the applications load different text fonts as needed, with the aid of the least recently used (LRU) algorithm. $175.

Graphics Software Systems, Box 673, Wilsonville, OR 97070. Phone (503) 682-1601. TLX 4994839.

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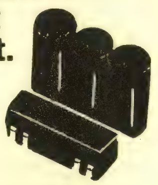

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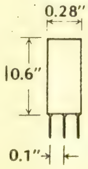

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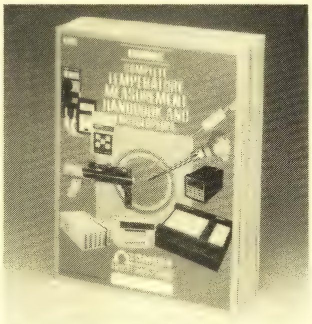

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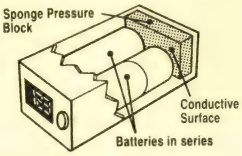

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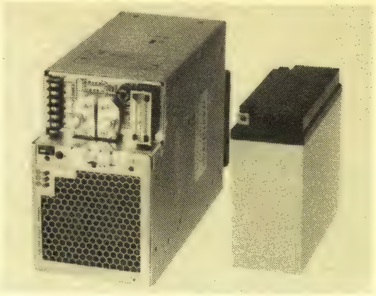

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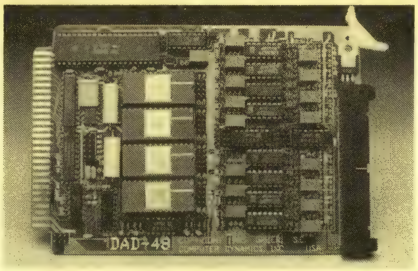

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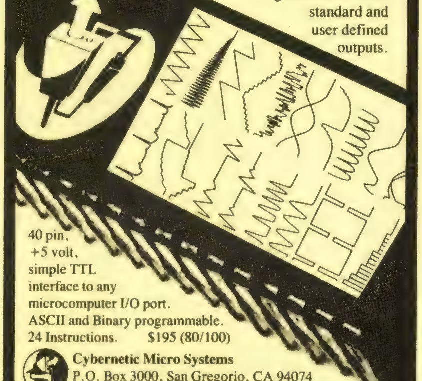

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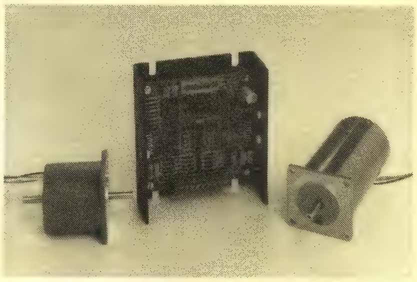

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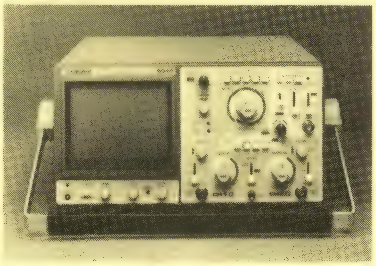

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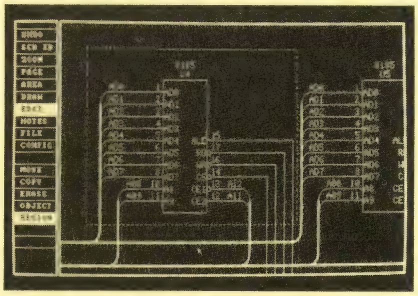

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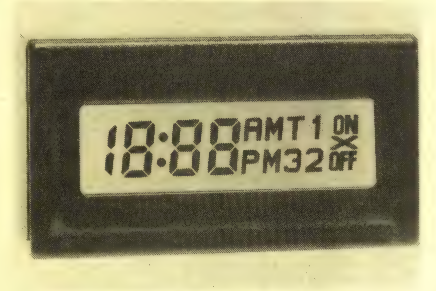

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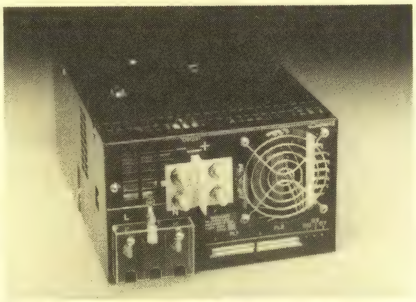

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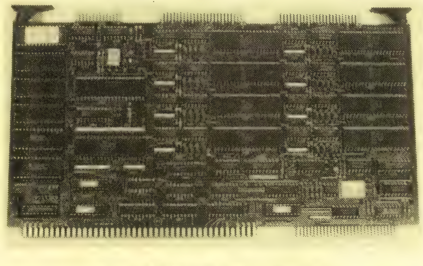

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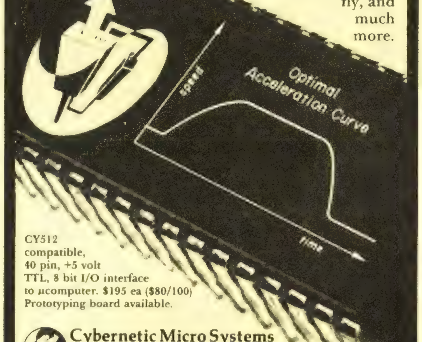

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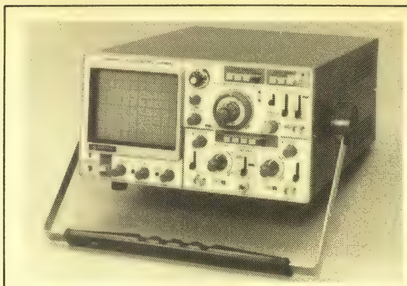

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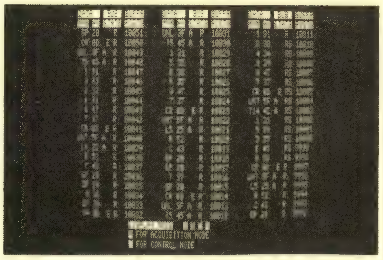

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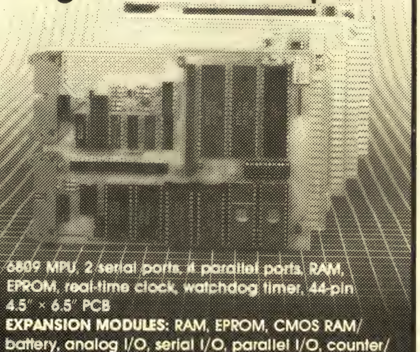

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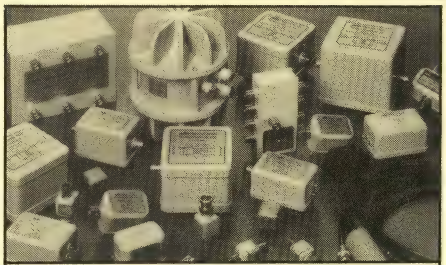

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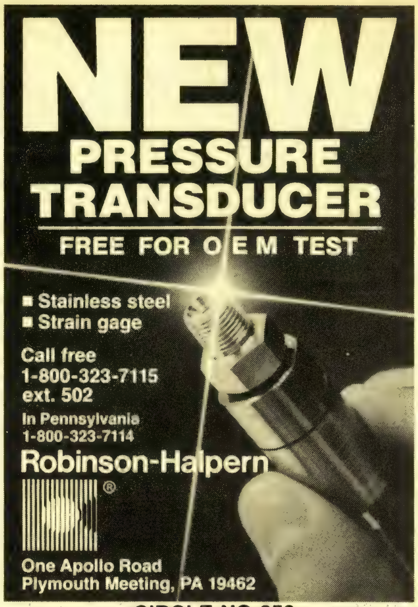

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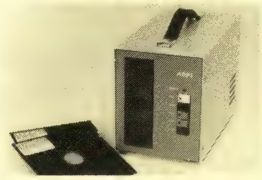

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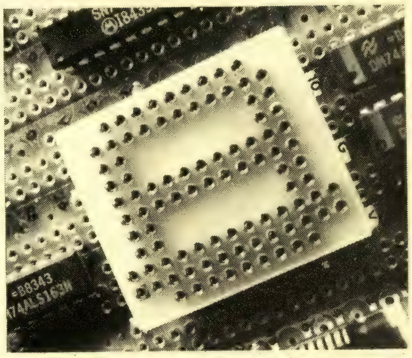

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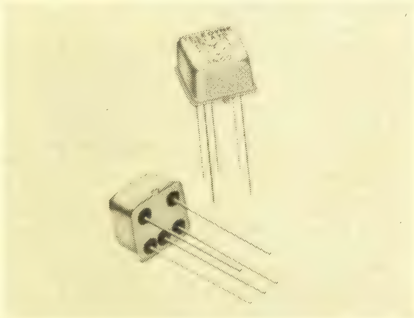

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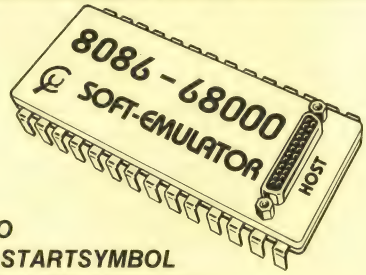

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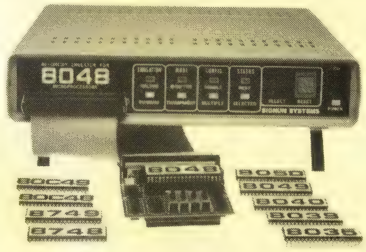

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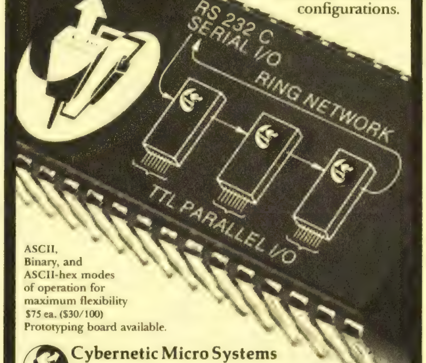

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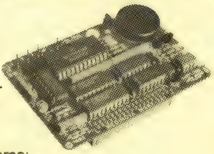

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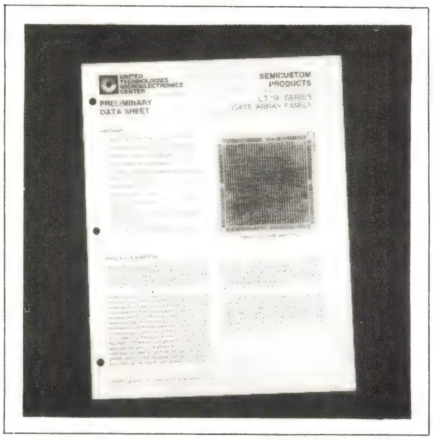

Data sheet features high-reliability arrays

Describing the B Series gate arrays, this 8-pg preliminary data sheet lists features and specs of the high-reliability parts. The text covers cells, macros, and buffers, as well as the manufacturer's design system and services. In addition, the publication uses tables to list electrical characteristics and includes line drawings of switching waveforms. Screening procedures are also described.

United Technologies, Microelectronics Center, 1575 Garden of the Gods Rd, Colorado Springs, CO 80907.

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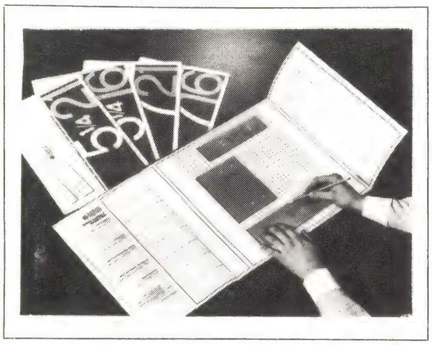

Design power modules

Using this kit of templates and layout grids, you can design power modules that provide 10 to 600W. The manufacturer will build the device a few weeks after you submit the design. The kit lets you design single- and multiple-output modules and switching or linear-programmable types. The full-scale templates let you design modules that fit into standard rack drawers. You can provide a front panel with as many as eight subpanels containing such devices as meters, LEDs, and circuit breakers. You can lay out the back panel with I/O connectors, barrier strips, or custom connectors. A pricing guide is included.

Kepco Inc, 131-38 Sanford Ave, Flushing, NY 11352.

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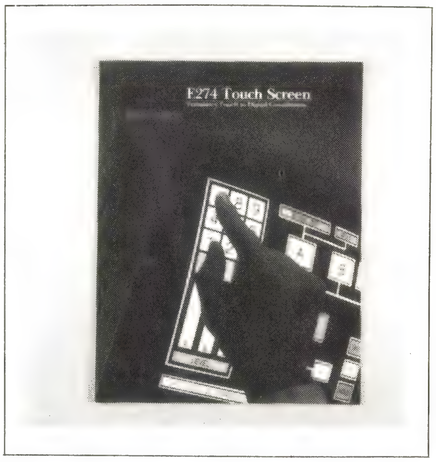


Touchscreen explained

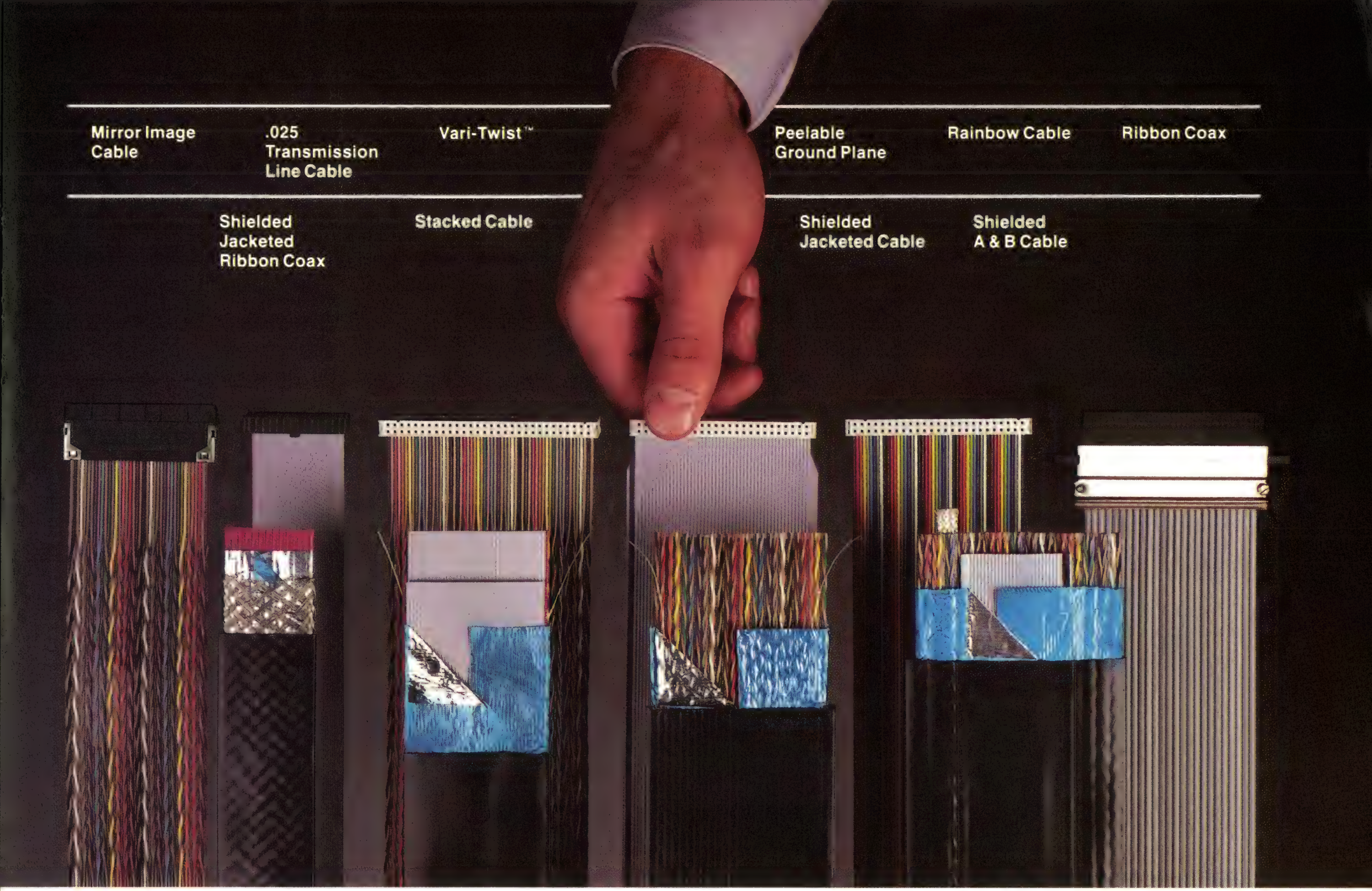
Applications, operation, and specifications of the E274 touchscreen are the topics of this 6-pg brochure. The document provides examples of touchscreen applications, describes the technology of the E274, and gives an analysis of its features and specs. The E274 suits both experienced and inexperienced users, according to the manufacturer.

Elographics Inc, 105 Randolph Rd, Oak Ridge, TN 37830.

Circle No 438

Guide covers transistor line

The manufacturer's Super E-Line (1W, TO-92) transistors are the topic of this 112-pg paperback guide. The document, organized in five sections, describes the prod-ucts' chip and packaging technologies, provides a product index of commercial and quality-assured products, and contains a selector table. It also provides technical



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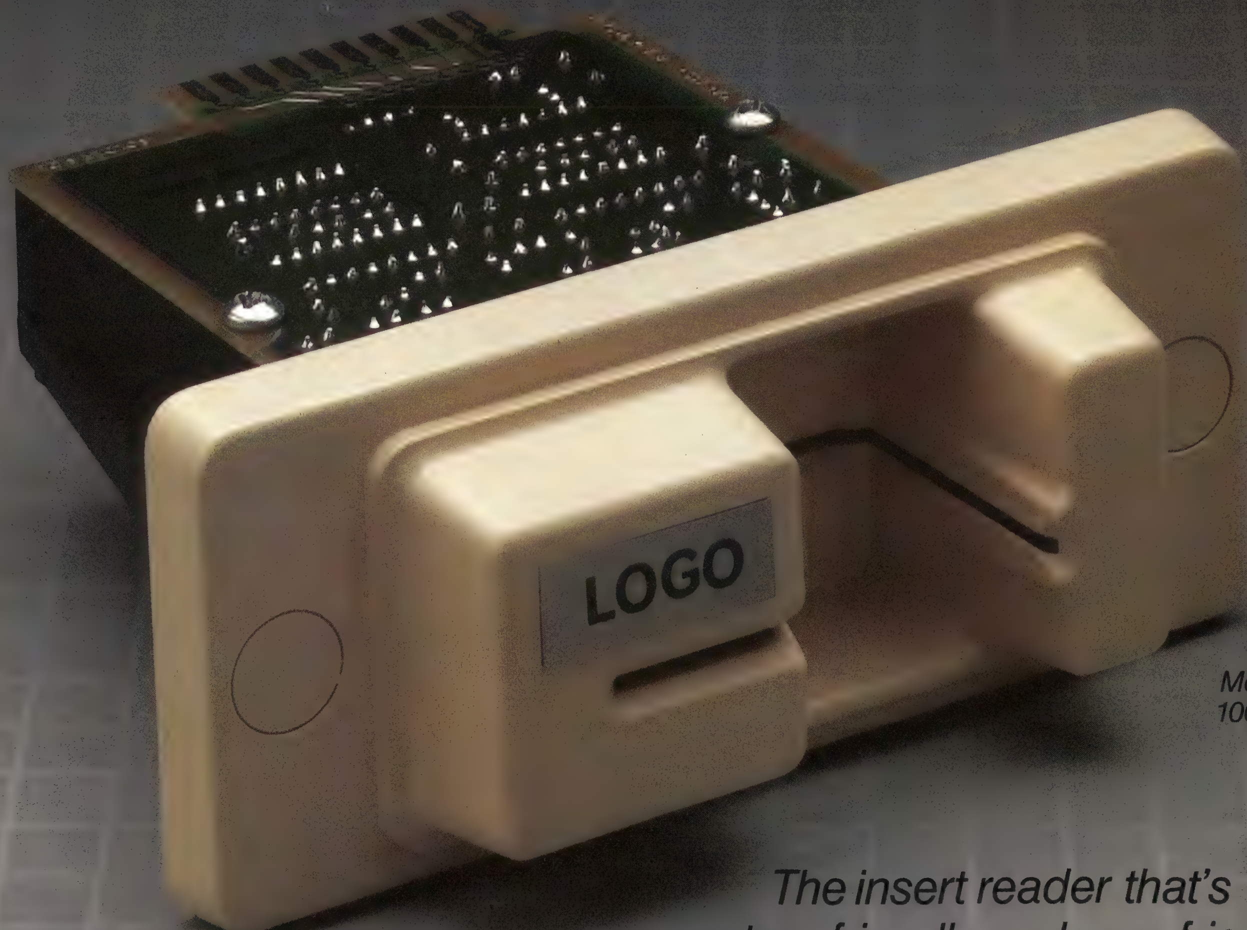

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CIRCLE NO 184

specs and application notes. The technical-data section contains fully characterized data on the devices, which spec breakdown voltages to 300V and collector currents to 2A continuous, 6A pulsed.

Ferranti Electric, Semiconductor Div, 87 Modular Ave, Commack, NY 11725.

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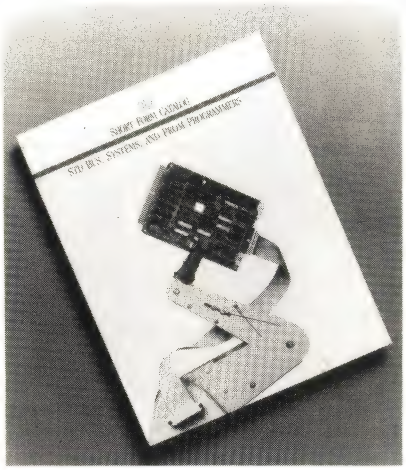


STD Bus μP cards described

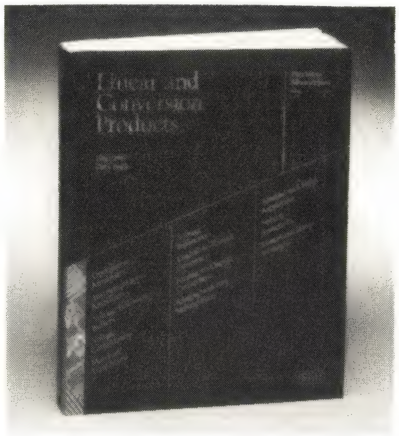
This short-form catalog describes the company's Series 7000 STD Bus μP cards. The 117-pg catalog also provides information on the company's IBM PC-based development and control systems. In addition to product features and pricing information, the catalog provides information on such recently released products as BWS Basic, a multitasking Z80 control system; SMDS, a single-master software-development system; and Multimasters, CPU-board products that allow as many as 16 8088 μPs to operate independently in an STD Bus-based system.

Pro-Log Corp, 2411 Garden Rd, Monterey, CA 93940.

Circle No 440

Book lists analog-IC devices

Linear and Conversion Products is an 896-pg data book for the vendor's



analog-IC products. Among the product families characterized in this 1986/1987 data book are op amps, instrumentation amplifiers, voltage followers/buffers, voltage comparators, matched transistors, voltage references, D/A and A/D converters, analog switches/multiplexers, and S/H amps. The book also describes special-function parts and communications products, and it gives ordering and packaging information.

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052.

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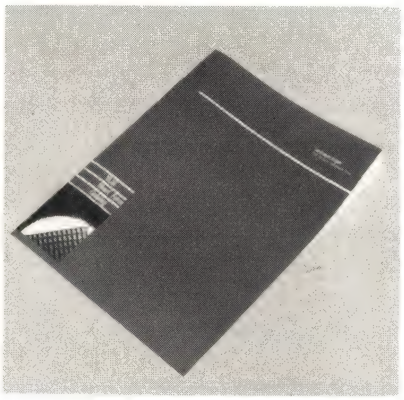


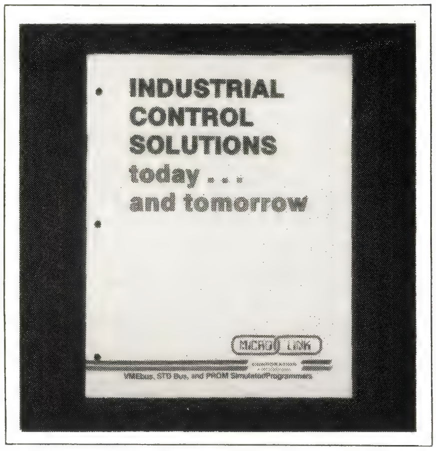
Converters, DSP components categorized

This 8-pg short-form catalog describes a line of VLSI high-performance converters and digital-signal-processing components; both CMOS and bipolar parts are included. The products are organized in six categories: A/D converters,

D/A converters, multipliers, multiplier/accumulators, memory/storage products, and special-function products.

TRW, LSI Products Div, Box 2472, La Jolla, CA 92038.

Circle No 442



STD and VME Bus products are characterized

This 36-pg catalog features more than 60 STD Bus and VME Bus microcomputer boards as well as firmware and support software and hardware. Among the products covered are single-board computers, CPUs, memory devices, and parts that perform I/O and communications functions. The products are based on the Z80, 8085, 68000, and 68008 μPs. Also described is the company's EPROM emulator/programmer family, Romaid. Rounding out the catalog is a section on value-added custom-board services and a tutorial section on the buses. Pricing information is not included.

Micro-Link Corp, 14602 N US Hwy 31, Carmel, IN 46032.

Circle No 443

Pamphlet features VME Bus hardware and software

Hardware and software VME Bus products are described in this 6-pg pamphlet. It covers 29 products, including a single-enclosure development system; 16-bit 1-board CPUs with speeds to 12.5 MHz; and memory boards with parity check-

ing or data security, which provide as much as 3M bytes of RAM. Other products include I/O and graphics controllers, hard- and floppy-disk units, backplanes, and power supplies. The software library features four operating systems and eight high-level languages, some of which are based in EPROM.

Plessey Microsystems, 1 Blue Hill Plaza, Pearl River, NY 10965.

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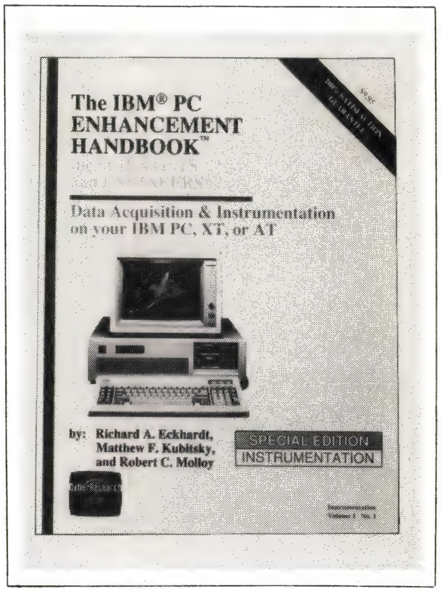

Handbook/catalog aids in IBM PC upgrades

The IBM PC Enhancement Handbook for Scientists and Engineers is a combination handbook and catalog that presents both tutorial information and descriptions of products. The special edition on data acquisi-

tion and instrumentation based on the IBM PC/XT and PC/AT describes technical products and integrated systems for data acquisition, instrumentation control, and process control. The instrumentation section of the book covers such topics as the control of laboratory and production instruments via the IEEE-488 bus or serial communications channels. The book also describes products that convert the PC to various laboratory instruments (eg, digital oscilloscopes), and it details both hardware and software products that you can use to build PC-based systems. $9.95.

CyberResearch Inc, Box 9565, New Haven, CT 06536.

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Catalog features power modules

Featuring a variety of electrical, mechanical, and thermal specs, this 96-pg catalog details the company's thyristor/diode power modules. The catalog provides circuit diagrams, dimension drawings, definitions, fuse recommendations, and ratings curves. Snubber networks and hardware are also described.

Semikron Inc, Box 66, Hudson, NH 03051.

Circle No 446

Brochure describes distributed-control system

This 12-pg full-color brochure introduces the Icon/1000, a distributed-control system for batch and continuous-control applications. Among the features described are the system's computer-aided process-engineering (CAPE) software. According to the manufacturer, CAPE provides an icon-graphics environment that permits a complex process application to be configured without conventional computer-language programming.

Data Acquisition Systems Inc, 349 Congress St, Boston, MA 02210.

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CIRCLE NO 186

Recent Department of Defense restrictions target open technical conferences

Deborah Asbrand, *Staff Editor*

The open exchange of information among engineers and scientists attending technical meetings is under fire by the Department of Defense and the military. Fearing that militarily sensitive information will find its way into the hands of foreign governments as a result of open technical meetings, the Department of Defense (DoD) has taken increasingly stringent measures to restrict the content of technical information presented at these meetings.

In January, the DoD set forth new guidelines pertaining to technical meetings and government clearance of technical papers. The most controversial aspect of the guidelines is the provision for a new category for technical sessions that discuss material that the DoD terms "unclassified but sensitive." The new category is a cross between the meetings sponsored by technical societies, which have always been open to anyone who wished to attend, and the classified meetings sponsored by the DoD, which require special clearance for attendance. Attendance at any sessions that fall into the category of "unclassified but sensitive" will be limited largely to US citizens.

The new policies cap several years of effort by Defense officials to check the open flow of technology that abounds at the hundreds of meetings technical societies sponsor each year. Technical societies view open meetings as an indispensable part of their members' efforts to advance technology. But to military officials, such conferences are leaky valves from which important technical data flows unregulated.

Michael McLaughlin

Conference restrictions

Military officials' mounting concern over the easy access to information at technical meetings has been evident in the flurry of restrictions they've placed on conferences in recent years. Citing export-control laws, officials of the armed services have disrupted several conferences by ordering last-minute deletions of papers scheduled for presentation:

- Six days before the International Test Conference was scheduled to begin in November 1982, Air Force officials notified organizers, through Texas Instruments (the employer of the authors involved), that they wanted three papers withdrawn from the conference agenda. After a series of negotiations with Texas Instruments and conference officials, Air Force officials withdrew their request.
- Shortly before the IEEE's 1983 National Telesystems Conference was scheduled to begin, Air Force officials ordered three words struck from a paper scheduled for presentation.
- In August 1983, Navy officials ordered the IEEE to delete a 6-pg paper from the already-published conference proceedings of the IEEE International Symposium on Electromagnetic Compatibility held in Arlington, VA. Confusion over proper review procedures and disagreement over whether the paper, entitled

"Electromagnetic-Pulse Hardening of Navy Ships," contained sensitive information contributed to the late decision to pull the paper from the proceedings. The Navy paid $4585 to have the paper manually sliced from the 1700 copies of the proceedings.

- In January 1985, Army officials ordered a paper describing an advanced radar system struck from a special issue of *Proceedings of the IEEE* after the material had been readied for printing. Military officials' disagreement over the paper's classification had delayed its clearance.

It wasn't until last April, however, that a confrontation arose that moved the scientific and technical community to action. Two weeks before the Society of Photo-Optical Instrumentation Engineers (SPIE) Technical Symposium East, Defense officials ordered the removal of 40 of the more than 200 papers scheduled for presentation. And in an action that foreshadowed what was to come, Defense officials advised conference organizers that they could present several of the 40 papers, which contained sensitive, but not classified, information, if attendance at these sessions was restricted to US citizens.

SPIE leaders agreed to the experiment in an effort to salvage the meeting. Under the watch of Defense representatives who coordinated the restricted sessions, attendees were required to sign documents informing them that public disclosure of the information was prohibited and that violators of the agreement were subject to prosecution under export-control laws.

Organizers of the SPIE conference say that restricting attendance at the sessions was a concession they did not want to make, but in view of the alternative—eliminating papers outright—it was the only plausible course. "We felt we had an obligation to our members and to the people attending," recalls Barry Johnson, chairman of the conference and 1987 SPIE president-elect. "They had no way of knowing—and we had no way of contacting them—that many of the papers were not going to be presented."

Holding restricted sessions "was the only way we could see to go, otherwise the meeting would have been a disaster," says Johnson. "We had already had one disaster several years before." A 1982 SPIE meeting in San Diego, CA, was left in disarray when Defense officials informed conference organizers on opening day that 117 of the 600 scheduled papers contained classified information and could not be presented.

Military officials have taken other, related actions to stem the flow of information they consider a threat to national security.

Controlling access to technical innovation is an issue the Defense establishment approaches with great resolve. In addition to reining in the scope of information available at technical conferences, military officials have taken a number of other, related actions to stem the flow of information that, in the hands of potential enemies, may pose a threat to national security. In August 1984, vice admiral Richard Miller wrote a memo criticizing two Naval radar engineers for divulging sensitive military information to students during classes the men taught at George Washington University.

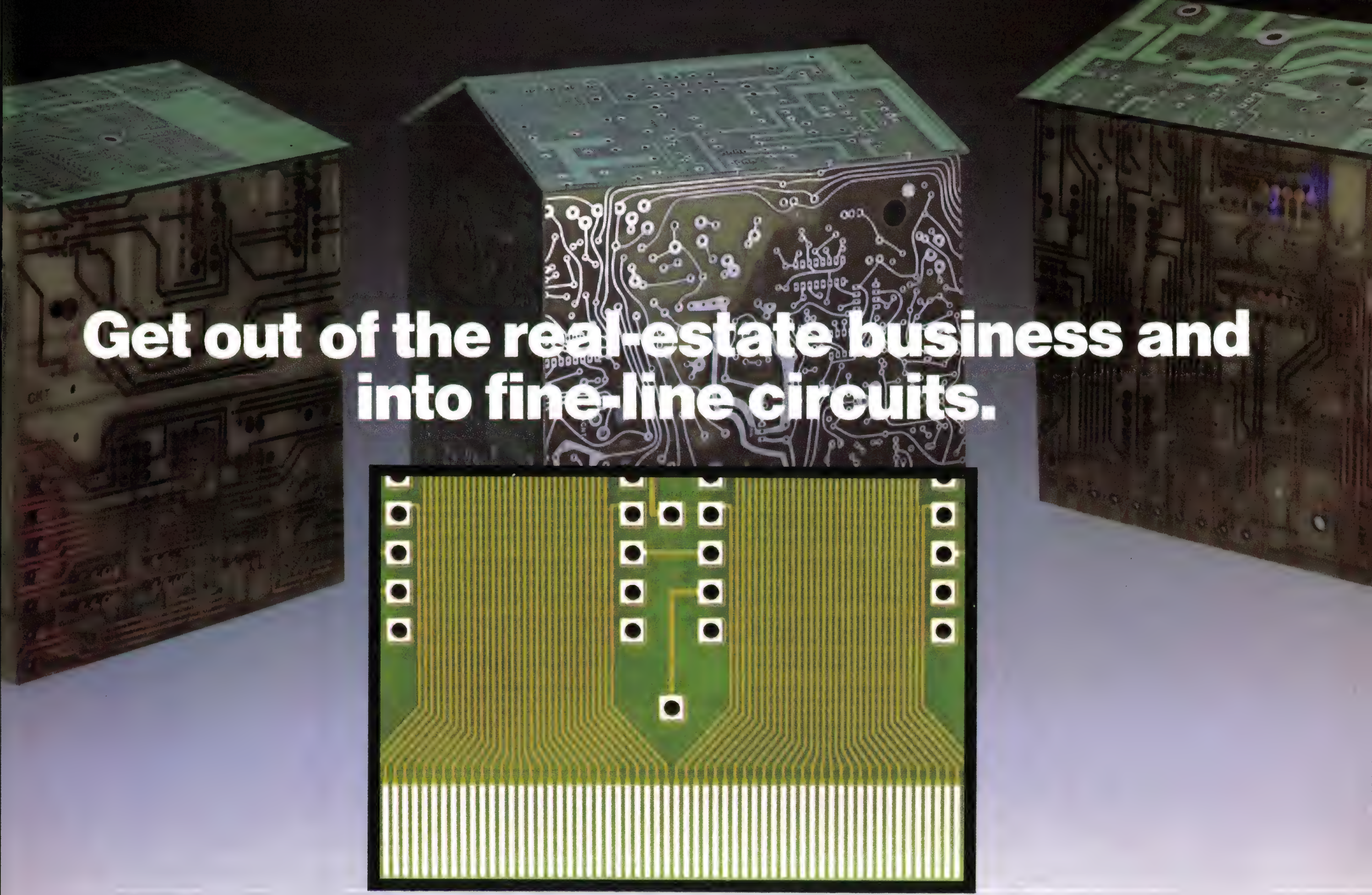
Last year, the Navy took another action, one that concerned IEEE leaders in particular. A June order directed the Navy's military and civilian personnel to reduce participation in nongovernment-sponsored technical conferences by 25%. The order stated that participation was to be reduced another 25% in fiscal year 1986.

The order, issued ostensibly as a cost-cutting measure, was of particular concern to the IEEE, many of whose members work in the military sector. "Our most recent survey of these members has shown a disturbing trend of job dissatisfaction," wrote 1985 IEEE president Charles Eldon in a letter to Navy Secretary John Lehman. "New sweeping restrictions on the ability of technical personnel to maintain their contacts with the cutting edge of their discipline will further exacerbate this trend" (see **box,** "Engineers rate conferences' educational value"). The Navy moderated its original order in September so that attendance at professional-society meetings was excluded from the cuts.

What these actions reflect, say society leaders, is the Reagan administration's belief that foreign nations benefit from the free exchange of technical information that exists in the United States. Moreover, the DoD worries that this openness threatens the US's ability to retain its technological edge in the world arena. Although previous administrations were equally concerned about the leakage of vital information to potential enemies, says Russell Drew, former IEEE vice president for professional activities, the Reagan administration is the first to impose limitations on the technical community. "This administration has broadened the definition of what vital information is and what should be controlled," says Drew. "It has applied controls to that information that previous administrations would not have [applied]."

The US-Soviet race

At the heart of the matter for the DoD is preventing US military rivals from obtaining technology that has military applications. In a letter last year to Senator James Abdnor (R-SD), Defense Secretary Caspar Weinberger wrote: "More than 5000



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CIRCLE NO 187

Soviet military research projects have benefited significantly, during the first half of this decade, from acquired Western technology. The West is subsidizing the Soviet military build-up."

A September 1985 DoD report on the Soviet acquisition of Western technology mentioned a conference of the IEEE's Aerospace and Electronic Systems Society as one of three conferences that, according to Soviet estimates, "produced savings of millions of rubles in long-range military research." The report did not specify the conference name, and the IEEE says it was unable to find out any further information about the conference referred to in the report.

The DoD under President Reagan gained an added measure of control over technical information through legislation passed in late 1984. The Defense Authorization Act closed a loophole in the Export Administration Act, the main body of legislation governing the export of information and goods. Although information controlled by the Export Administration Act had always been restricted, access to it could still be obtained under the Freedom of Information Act. With passage of the Defense Authorization Act, technical information that's generated through defense contracts is no longer accessible using the Freedom of Information Act. The 1984 act, says Drew, was the stimulus for the "new guidelines in which [Defense officials] started taking a much harder line on information dissemination."

Concern is misguided

Society leaders believe the government's concern with preventing the export of information through technical meetings is overstated. They argue that the free flow of information in the US is what contributes to this country's technological superiority. "Some parts of the Department of Defense operate from the standpoint that the US is the sole source of technology and keeping our barriers up will prevent the Russians from getting it. That's a myth," asserts Karl Willenbrock, former chairman of the IEEE Technology Transfer Committee. "There's good technology everywhere. We give but we also gain from a free interchange of information."

At the heart of the matter, the Department of Defense is preventing the US's military rivals from obtaining technology that has military applications.

Bob Park, executive director of the American Physical Society, says the administration's concern with information controls is misguided. "One has to ask why it is the Soviets have to steal our technology. It's my belief that the principal reason is that they have the same controls over there that [the Department of Defense] is trying to impose over here," says Park. "It shuts down their system so badly that it requires them to look to us for their technological developments. I find that highly reassuring. You can't be ahead if you're doing that; it guarantees they're in second place."

Technical societies object to the new guidelines, and the limited-access-meeting category in particular, for reasons of practicality as well as principle: Foreigners and foreign nationals in the US constitute a large chunk of many societies' memberships. Conference sessions limited to US citizens will potentially shut out large numbers of attendees. For example, of the SPIE's 6000 members, approximately 1200 are foreign nationals. For the IEEE, the restrictions present a problem of greater magnitude. Because the IEEE's membership roster contains 50,000 foreign members, says Willenbrock, the restricted sessions present "a fundamental conflict" for the society.

Societies reject proposal

Society leaders had the opportunity to air their views in a series of meetings with Defense officials last summer. By all accounts, the meetings proved to be a successful forum that allowed participants to voice their concerns and to resolve some outstanding matters.

Nevertheless, the Defense officials' proposal for restricted-access sessions at technical meetings—

Engineers rate conferences' educational value

Engineers indicate they have more than just a passing interest in technical conferences. In the 1984 IEEE Lifelong Education Survey, 78% of the respondents who believe that keeping abreast of technology is essential to their jobs indicated that conferences carry a strong or moderate importance in their efforts to remain up to date. Respondents do consider technical publications and job assignments better educational tools than technical conferences, however. Nonetheless, 49% of respondents noted that attendance at technical conferences had strongly or moderately increased in the three years prior to the survey. Thirty-nine percent of the respondents indicated that technical conferences' importance in remaining technically up to date had not changed, and 19% reported that the conferences' educational use had declined.

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CIRCLE NO 189

first experimented with at the April 1984, SPIE meeting—was overwhelmingly rejected by society representatives. In a joint letter to Weinberger in September 1985, the presidents of 12 technical societies reiterated that they did not concur with the DoD's restricted-access-meeting category. "Therefore our organizations will not be responsible for, nor will they sponsor, closed or restricted-access technical sessions at meetings or conferences conducted under their auspices," the letter read.

Defense representatives say that the issue of restricted-access sessions is a difficult one for their own department as well as for technical societies. "We're trying to keep technical conferences as open as they have been in the past," says Leo Young, director for research and laboratory management in the Office of the Secretary of Defense. "But at the same time, we do have concerns about what might be getting out needlessly."

Under the new guidelines, some papers submitted for review for military clearance may be marked for limited access only. Should the sponsoring societies choose to keep papers designated for limited access on the conference agenda, they have the option of turning over to Defense officials the responsibility for coordinating the session. Young, who acted as the DoD's liaison in the meetings with society leaders, says that he doesn't expect that the new limited-access-meeting category will be used often by the coordinators of technical conferences, but at least they'll have the option. According to Young, "What we're saying to societies is that if you want to make use of this [category], we will help you."

A more positive result of the societies' meetings with Defense officials concerns new clearance procedures for technical papers. Lengthy and unclear channels for reviewing technical papers were blamed for many of the last-minute raids that had disrupted recent technical conferences. Young says that prior to the new regulations, there were no deadlines for reviewing the nearly 2000 papers submitted for clearance each year, only "internal target times."

The new procedures, says Young, require the cooperation of three parties: the Department of Defense, which must take a timely, common-sense approach to identifying which material can be published; authors, who must allow enough time for the papers to be reviewed; and technical societies, which must know the proper channels and contacts for review.

As the DoD and the armed services flex their muscles, some society leaders worry that the open exchange of technical information among scientists and engineers remains threatened.

The new regulations require that military officials review material of a classified nature, and of an unclassified but limited nature, within 30 working days. In addition, authors may submit papers intended for presentation at unclassified, unlimited-attendance sessions, and such papers must be reviewed within 20 working days. The new regulations clearly delineate the responsibilities of the reviewing officials. Not always so clear, however, are authors' responsibilities.

Long arm of the government

Stipulations in their employers' government contracts govern the publishing activities of authors whose papers are stimulated by classified work. But authors of papers that result from unclassified work have no such guidelines. In these cases, says Young, it's up to the individuals to decide whether they want the papers reviewed for clearance. Although authors of unclassified technical papers are not required to submit their work for review, Young warns that the arm of the government is long: Authors who present unreviewed technical material that military officials later deem classified or sensitive can be prosecuted by the Justice Department for violation of export-control laws.

By voluntarily submitting unclassified papers for review, Young says, authors relieve themselves of any responsibility for the material. After a paper has been reviewed for clearance, responsibility for its contents shifts to the DoD.

Young says he is satisfied that the new regulations strike a balance that allows the DoD to secure militarily sensitive information and that also permits technical meetings to proceed for the most part unhindered. "I think [the guidelines] we've come up with are sensible," he says. "They state the obvious in a way, but it's good to have them written down."

"Counterproductive" controls

Yet some society leaders continue to worry that the open exchange of technical information among scientists and engineers remains threatened. Although Bob Park of the American Physical Society believes society leaders successfully persuaded Defense officials to modify their original stance, he calls the controls "counterproductive." National security, he says, depends on technological progress rather than technological controls.

Others say the character of technical meetings could change if restrictions continue to be imposed. "I fear that if there's a strong push by the Department of Defense to broaden the net of what is sensitive material, the quality of meetings will go down," says the SPIE's Johnson.

Lewis Larmore, the society's 1985 president, calls the new re-

stricted-access-meeting category "another roadblock in the dissemination of information in our country." His predictions for the future of technical meetings are more ominous: Before the character of the meetings has a chance to change, he says, "they may be abolished."

Coincidentally, the new procedures' first test will occur later this month at the spring meeting of the Society of Photo-Optical Instrumentation Engineers—the event at which the DoD first experimented with restricted-access sessions last year. "SPIE is in an awkward situation," admits Young. "When you get into electro-optics, there are many systems that are unclassified, and yet the military applications are quite obvious. We don't want the Russians to be there writing it all down."

Although restricted sessions will be held, SPIE is on record opposing such sessions. (Lewis Larmore, the SPIE's 1985 president, was among the society leaders who signed the letter to Weinberger relinquishing responsibility for such sessions.) The organization is publicizing the existence of the meetings as a courtesy to attendees, says Barry Johnson.

The real issue comes down to weighing the potential for loss of information against the progress of technology in the US. How important are open meetings to technological progress? Johnson responds by posing another question: "What is the growth of science and technology like in countries where information is suppressed and controlled, compared with countries where there is free and open enterprise? You answer the question." **EDN**

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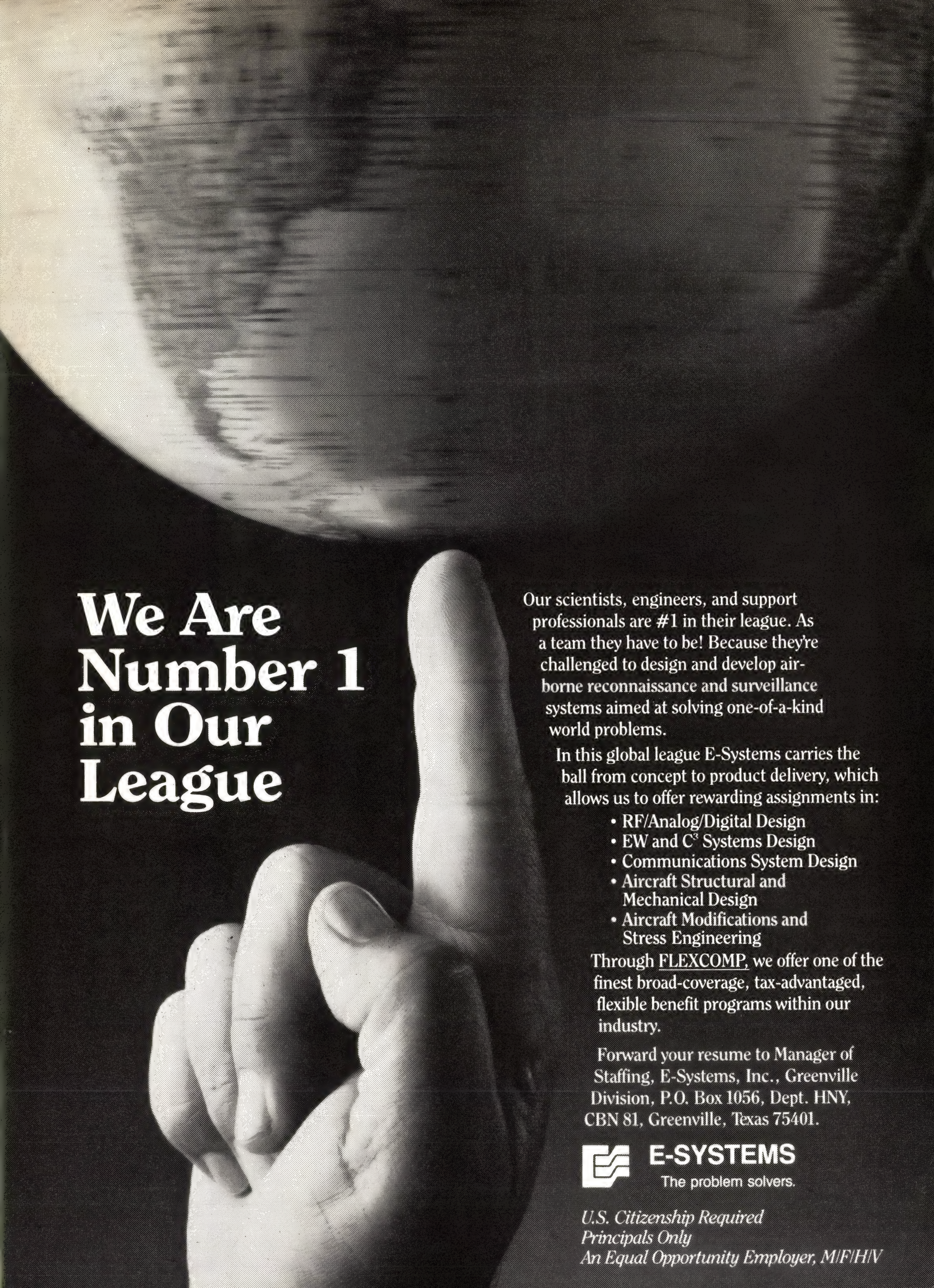
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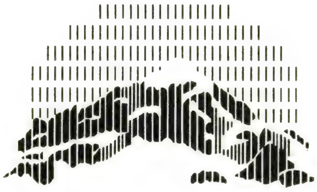

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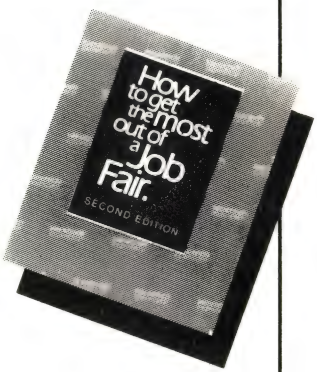

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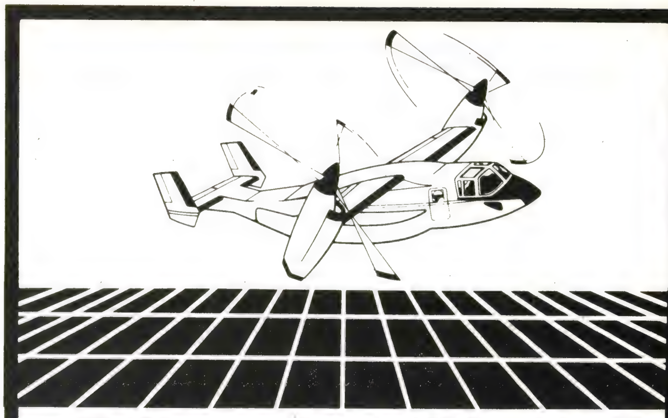

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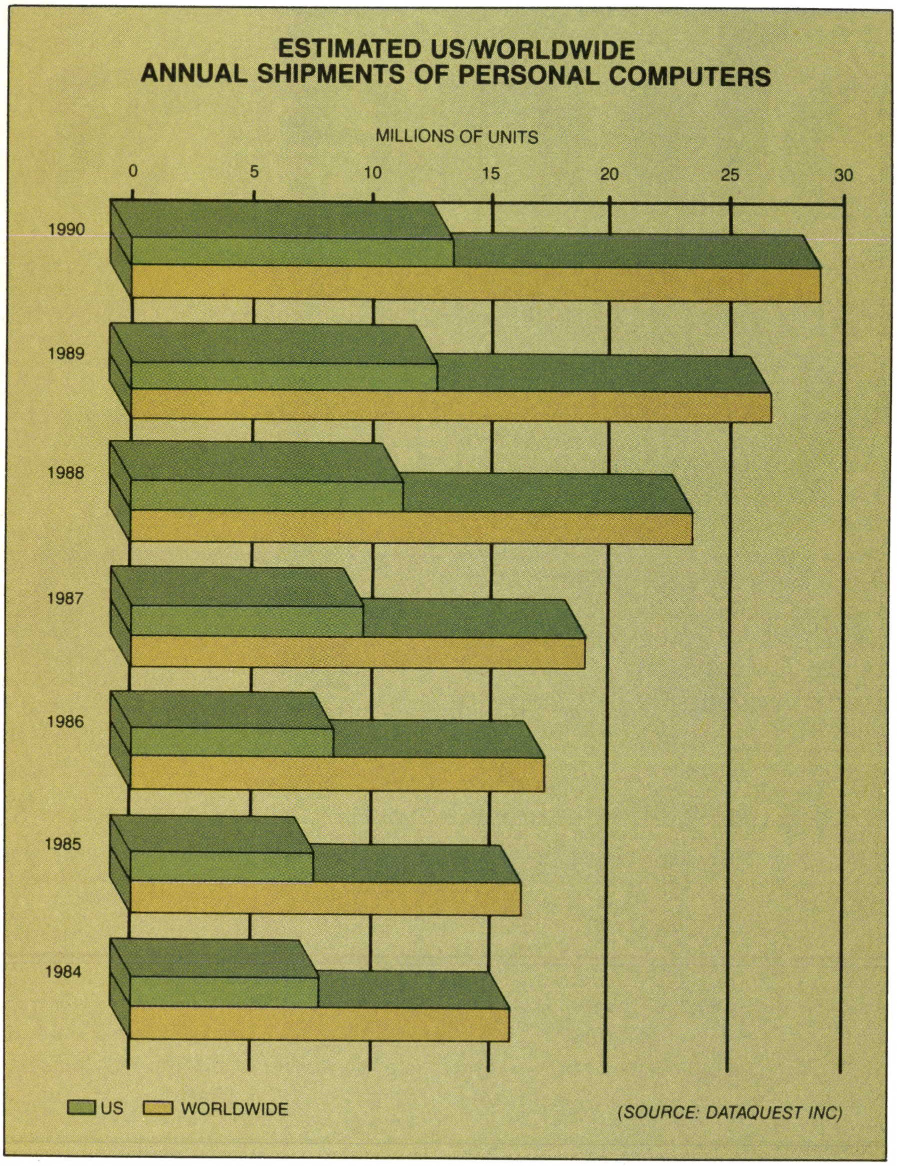
EDITED BY GEORGE STUBBS

Personal-computer market to grow slowly in 1986

Although it regards the personal-computer industry as "holding up well," the market-research company Dataquest Inc (San Jose, CA) believes the growth rate of the industry will continue to decline in 1986, in terms of dollar value of units sold. Growth figures for units shipped and dollar value were 3.6% and 31.6% in 1985, respectively. The respective 1986 figures, projected to be 5.4% and 7.8%, are a far cry from 1984's 46% and 73% tallies.

Dataquest attributes the low growth rate to cutthroat price competition among surviving vendors and "fire-sale prices" from desperate companies. Yet the industry might not be in such dire straits as is often assumed: Only a few companies went out of business in 1985, while a few dozen entered the market.

Forecasts for the longer term show steady growth in shipments of personal computers. In 1987, approximately 9 million units will be sold, and by 1990 that number will be about 13 million. The worldwide figures for the same two years range from approximately 19 million units to better than 28 million units.



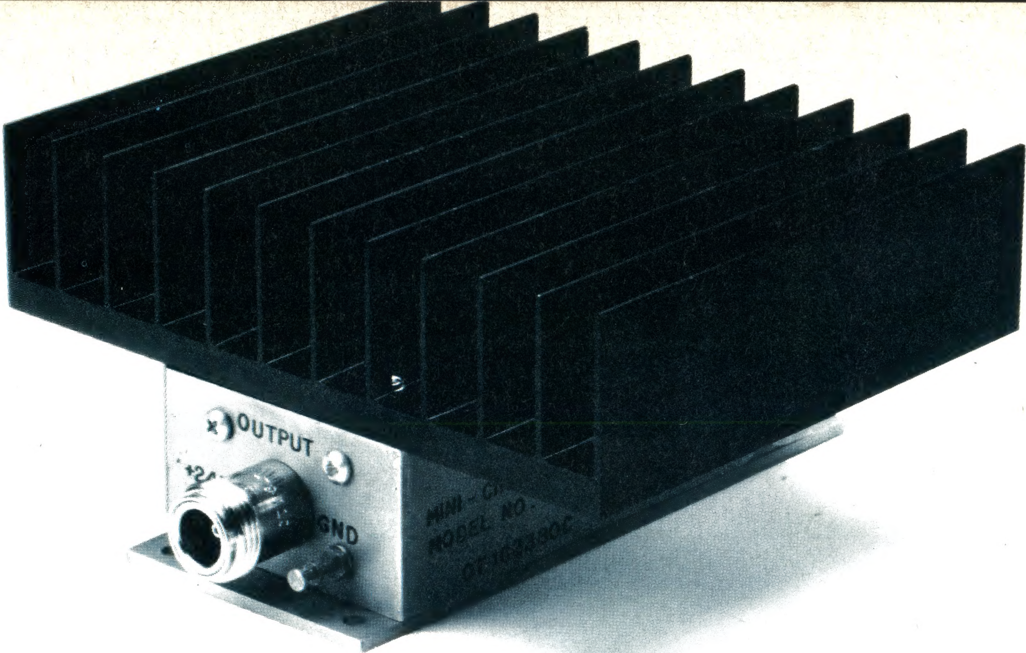
Databases to streamline infrastructure management

City hall may soon be running out of excuses. If automated-mapping/facilities-management (AM/FM) databases catch on, public utilities, public-works departments, and local governments will have immediate access to information regarding the location and condition of various elements of the infrastructure, such as streets, water mains, and power lines. They will also be able to find out who has responsibility for such elements. According to the editorial staff of the *F-M Automation Newsletter* (Rosemont, IL), these AM/FM databases present a significant applications opportunity for vendors of personal-computer-based CAD systems and for other segments of the computer industry.

Estimates of the potential market for AM/FM systems range from $50 billion to $100 billion. The databases represent somewhat of a departure from traditional data-storage techniques in that they will contain information in the form of positions on maps as well as in more conventional recording formats.

The market opportunities fall into two general groups. First, consultants; specialists in various fields (land surveying, civil engineering, computer programming, etc); and data-conversion service providers will prepare the digital databases of maps and other information that public utilities and local government departments need.

Second, there will be opportunities for manufacturers of hardware and software, who will provide systems for AM/FM data conversion and for AM/FM database operation. These vendors include suppliers of CAD workstations, image-processing systems, mass-storage devices, computers of all sizes, printers and plotters, machine-vision systems, networking and telecommunications systems, controllers, and software for all system levels.



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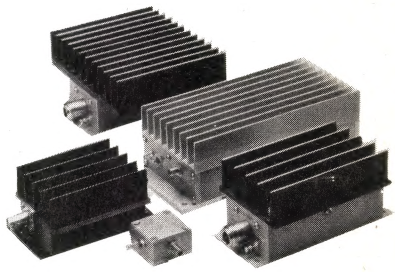

Model No.	Freq. MHz	Gain dB	Gain Flatness dB	Max. Power Output 1dBm Compression	Noise Figure dB	Intercept Point, Typ. 3rd Order	DC Power Voltage	DC Power Current	Price $ Ea.	Price Qty.
ZHL-32A	0.05-130	25 Min.	±1.0 Max.	+29 dBm Min.	10 Typ.	+38 dBm	+24V	0.6A	199.00	(1-9)
ZHL-3A	0.4-150	24 Min.	±1.0 Max.	+29.5 dBm Min.	11 Typ.	+38 dBm	+24V	0.6A	199.00	(1-9)
ZHL-1A	2-500	16 Min.	±1.0 Max.	+28 dBm Min.	11 Typ.	+38 dBm	+24V	0.6A	199.00	(1-9)
ZHL-2	10-1000	15 Min.	±1.0 Max.	+29 dBm Min.	18 Typ.	+38 dBm	+24V	0.6A	349.00	(1-9)
ZHL-2-8	10-1000	27 Min.	±1.0 Max.	+29 dBm Min.	10 Typ.	+38 dBm	+24V	0.65A	474.00	(1-9)
ZHL-2-12	10-1200	24 Min.	±1.0 Max.	+29 dBm Min.	10 Typ.	+38 dBm	+24V	0.75A	599.00	(1-9)
ZHL-1-2W	5-500	29 Min.	±1.0 Max.	+33 dBm Min.	12 Typ.	+44 dBm	+24V	0.9A	495.00	(1-9)
ZHL-42	**700-4200**	30 Min.	±1.0 Max.	+29 dBm Min.	7.5 Typ.	+38 dBm	+15V	0.69A	895.00	(1-9)
ZHL-7-2W	600-800	28 Min.	±1.0 Max.	+33 dBm Min.	12 Typ.	+43 dBm	+24V	0.9A	525.00	(1-9)
ZFL-2000	10-2000	20 Min.	±1.5 Max.	+17 dBm Min.	7 Typ.	+25 dBm	**+15V**	0.1A	179.00	(1-9)

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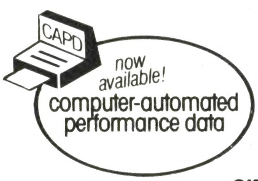

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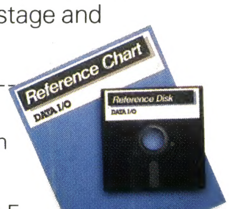

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